PROCEEDINGS OF SCIENCE

A DEPFET vertex detector for the linear e^+e^- collider

Marcel Vos[*†]
IFIC (UVEG/CSIC) Valencia, Spain
E-mail: marcel.vos@ific.uv.es

The DEPFET collaboration develops highly granular, ultra-transparent active pixel detectors for high-performance vertex reconstruction at future collider experiments. In this contribution I present a vertex detector design for a future linear $\mathbf{e}^+\mathbf{e}^-$ collider at the energy frontier and show that the expected performance satisfies the stringent requirements of the experiments.

22nd International Workshop on Vertex Detectors,
15-20 September 2013
Lake Starnberg, Germany

[*]Speaker.
[†]On behalf of the DEPFET collaboration (www.depfet.org).

PoS(Vertex 2013)023

1. Introduction

A lepton collider can provide valuable precision measurements of Standard Model processes. An electron-positron machine with a center-of-mass of approximately 250-350 GeV and an integrated luminosity of at least an inverse attobarn can measure the couplings to Standard Model particles of the Higgs boson discovered in 2012 [1, 2, 3] with excellent precision. Higher-energy operation allows access to vector-boson-fusion production, Higgs production in association with a top quark pair ($t\bar{t}H$) and double Higgs boson production. A more detailed account is found in another contribution to these proceedings [4]. Further benefits of such a machine include detailed measurements of top quark properties [5] and a sensitivity to physics beyond the Standard Model that complements the strengths of the LHC [6].

To perform this precision physics program experiments at a future linear e^+e^- collider (LC) require very precise reconstruction of the reaction products. Key figures of merit for the detector performance, such as the jet energy resolution, momentum resolution for charged tracks, and the vertexing capabilities of the experiment, must be improved significantly with respect to the state-of-the-art detectors realized in the LHC experiments or those under development for a future luminosity upgrade. A worldwide detector R & D effort is ongoing to fully satisfy these challenging requirements.

Finely segmented solid state detectors are crucial for the reconstruction of the trajectory of charged particles in modern collider experiments. Over the last decade an international collaboration has developed the DEPFET (Depleted Field Effect Transistor [7]) concept, where a FET is integrated in the sensor to amplify the signal. These DEPFET structures present interesting possibilities for a number of applications. The excellent signal to noise (S/N) ratio that can be achieved has led to applications such as space-based X-ray Astronomy missions and X-ray detection in the European XFEL [8].

The internal amplification of DEPFET sensors also allows for a strong reduction of the material budget of position-sensitive devices for charged particle detection at collider experiments. The proposal of a DEPFET vertex detector for a future linear e^+e^- collider [9, 10] dates back to 2002. In 2010 DEPFET technology was selected for the vertex detector of the Belle II experiment at the upgraded KEKB B-factory in Japan, that is to start operation in 2016. The progress of the DEPFET collaboration towards a fully engineered detector design and the prospects for production are presented in another contribution to these proceedings [11]. In this contribution I present the design of a DEPFET-based vertex detector for a future experiment at a (linear) e^+e^- collider at the energy frontier. I discuss recent advances in the light of the requirements of such a machine. A more detailed and complete discussion is found in Ref. [12].

2. Ladder concept

In the ILC experiments, five or six DEPFET pixel detector ladders are to be oriented parallel to the beam line, with the first layer at a radius of 15 mm. The ladder design for the innermost layer of the ILC barrel vertex detector is schematically depicted in Figure 1. The core of the ladder assembly is formed by two DEPFET sensors that are joined in the center. Over most of the sensor area they are thinned to 50 μm using a novel thinning concept [13, 14]. Several thicker areas are

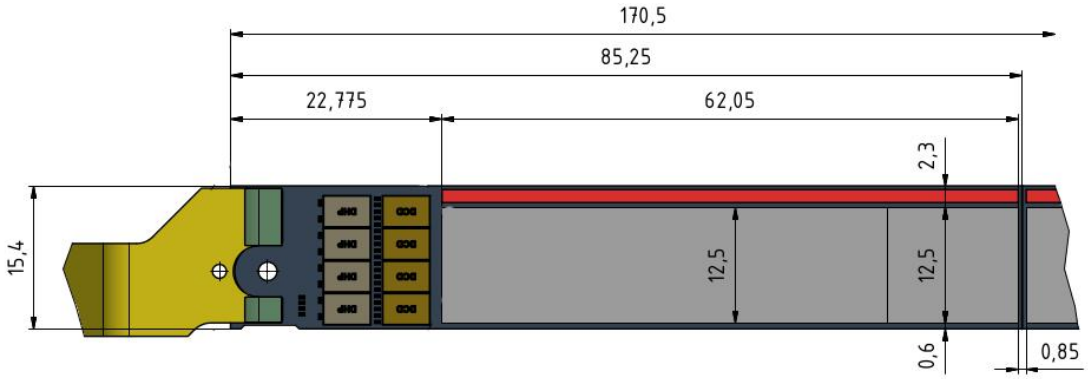

Figure 1: Schematic ladder layout for the innermost layer of an LC vertex detector. The end-of-ladder area that houses the read-out ASICs is visible on the leftmost side of the figure. The active area is indicated in light grey. The balcony that houses the control electronics is seen on top of the picture, running along the full length of the sensor. Dimensions are given in millimeters.

kept at the end-of-ladder, the edge of the sensor and the balcony that carries the steering ASICs, forming a rigid mechanical frame. The all-silicon concept thus yields a self-supporting ladder with a minimal material budget.

Pixels in the center of the sensor are 25 $\times$ 25 μm^2. The pixel dimension in the z-direction (along the beam line) is varied over the length of the sensor, ensuring that charge is shared over a small number of pixels independent of the z-position. The pitch is increased to 50 μm at $|z| = \pm$ 1 cm and to 100 μm at $|z| = \pm$ 2 cm. Two early sensor production batches have proven the feasibility of small pixels down to 20 $\times$ 20 μm^2. The performance of the ILC prototypes constructed with these sensors is described in several previous publications [15, 16]. Larger pixels are envisaged for Belle II. Prototypes with thinned sensors have been extensively tested (see Refs. [17] and [11]).

The DEPFET pixels are organized in columns that stretch along the length of the sensor. Each column is read out by a single channel of the DCD chip (Drain Current Digitizer [18, 19, 20, 21]) locate at the end-of-ladder. The DCD analog input stage keeps the column line potential constant and compensates for variations in the DEPFET pedestal currents. A transimpedance amplifier amplifies and shapes the signal. The analog signal is digitized using two 8-bit current-mode cyclic ADCs with a sampling frequency of 10 MSamples/s. The DCD can be operated in double correlated sampling mode or single sampling mode. The latter is preferred as it allows higher read-out speed. The DCD is implemented in UMC 0.18 μm CMOS technology using special radiation hard design techniques (e.g. enclosed NMOS gates) in the analog part. The 256-channel DCDB, with an area of 3.2 $\times$ 5 mm^2, optimized specifically for Belle II requirements, is fully functional at the nominal 320 MHz. Radiation tolerance of at least 70 kGy has been proven.

The SWITCHER control chips are located on a narrow balcony that stretches along the length of the ladder. SWITCHERs select segments of the sensor (pairs of rows or 4-row segments) for read-out. A separate driver supplies the *clear* pulse of up to 20 V to remove the collected signal from the internal gate after read-out. Two designs of the SWITCHER versions optimized for Belle II requirements (SWITCHERB18 in 0.18 μm and SWITCHERB in 0.35μm) have been produced and tested successfully. These ASICs can produce pulses with a maximum swing of 20 V

in a voltage range of 50 V. Measurements show that the current SWITCHER chips can drive long lines, up to loads well beyond the requirements of the Belle II and LC vertex detectors.

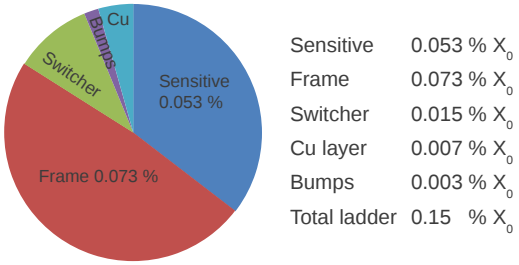

Figure 2: Break-down among the detector components of the material expressed in units of radiation lengths over the acceptance of the all-silicon ladder design.

The detailed ladder design for an LC vertex detector envisages a contribution to the detector material (averaged over the ladder area) that is equivalent to $\sim 0.15\%$ X_0/layer. A break-down of the material among the components with the most important contributions is presented in Figure 2. The basis of this estimate is the fully engineered Belle II design [17], that corresponds to 0.21% X_0/layer over the active area. The LC budget is reduced primarily by a more aggressive thinning of the sensor. The thickness of the active material, one of the dominant contributions, is reduced from 75 μm to 50 μm (as already achieved in the Belle II prototype production run). The support frame is reduced from 450 μm to 400 μm.

3. S/N ratio

Minimum Ionizing Particles (MIPs) deposit a small signal in thin layers of silicon: for a 50 μm thick sensor the typical signal is approximately 4000 electrons. To find the particle signal with good efficiency and improve the resolution by interpolating between the signal of neighbouring pixels, the signal must be well above the electronics noise. DEPFET sensors achieve a comfortable S/N ratio with a very thin sensor by integrating a Field Effect Transistor in each pixel, that amplifies the small signal. The gain of this first stage is a key parameter of the system. Prototypes have achieved gains of 300-700 pA/e^- [17]. The range of values is due to variations in the layout of the FET. The analysis in Ref. [12] of gain measurements on single-pixel structures [22, 23] show that the relation predicted by a simple 2D model between the gain and the the length of the gate L, its width w and the oxide thickness t_{ox}, and the drain-source current I_{ds}.:

$$g_q \propto \frac{I_{ds}^{1/2} \times t_{ox}^{1/2}}{w^{1/2} \times L^{3/2}} \tag{3.1}$$

provides an adequate rule of thumb for not-too-large values of the current.

Measurements of the DCDB noise yield 80 nA for a capacitative load of 80 pF, that corresponds to a full-length DEPFET ladder [21, 24]. The response of complete read-out modules built around DEPFET sensors from the PXD5 and PXD6 production has been characterized in beams of charged particles from accelerators at CERN and DESY [15, 16, 25, 26]. The first set of measurements is on 450 μm ILC-design sensors with pixel sizes ranging from 20 $\times$ 20 μm^2 to 24 $\times$

32 μm^2. The read-out module for these prototypes relies on the CURO chip [27, 28]. More recent measurements correspond to thinned PXD6 sensors with DCDB read-out.

The DEPFET drain current distributions due to perpendicularly incident 120 GeV pions from the CERN SPS are shown in Figure 3. The upper panel corresponds to a 450 μm thick "PXD5" sensor and the lower panel to a PXD6 sensor thinned to 50μm. The signal in adjacent pixels is added using a simple clustering algorithm with a neighbor cut of 2.6 σ. Further details of the analysis can be found in Reference [29]. Both measurements are corrected for the measured gain of the Front End ASICs[1]. To facilitate comparison the results are moreover divided by the sensor thickness.

The measurements are compared to the prediction for the energy deposition in thin silicon layers of H. Bichsel [31]. The predicted energy deposition is converted to signal per unit thickness by dividing by the ionization potential of silicon (3.62 eV). The internal gain of the sensors is left floating. The quantum gain g_q of the sensors thus obtained (340 pA/e^- for the 450 μm thick sensor, in good agreement with the result of a calibration with a γ source, and 470 pA/e^- for the thin sensor). Both results are in good agreement with the expected gain [12]. These results show that thin DEPFET ladders (down to 50 μm) can indeed achieve a comfortable S/N ratio of over 40.

Also the shape of the distributions is in good agreement with the model prediction. In particular, the model correctly reproduces the broader signal distribution observed for the thin sensor: The peak position divided by the Full Width at Half Maximum (FWHM) yields: $\Delta_p/w = 1.67$ for the 50 μm sensor (prediction: 1.61) and $\Delta_p/w = 3.06$ for the 450 μm thick sensor (prediction: 3.13).

Finally, the uniformity of the signal over the area of the sensor has been evaluated. The channel-to-channel variation of the ADC conversion factor in the DCDB is found to be approximately 2% [24]. Variations in the response to MIPs measured at the beam test, including also non-uniformities in the sensor response, are below 5%, at which level they are expected to have a negligible impact on the overall detector performance.

4. Read-out speed

The read-out speed is one of the most challenging requirements of the LC vertex detector. The first layer of the LC vertex detector must cope with a large background of charged particles due to incoherent e^+e^- pair production. For the International Linear Collider with $\sqrt{s} = 500$ GeV a background hit density of up to 10 hits/cm^2/μs in the innermost layers of the vertex detector at 15 mm from the interaction point. Pattern recognition and unambiguous cluster reconstruction require read out times of 50-100 μm and a highly granular detector [32, 33].

The background hit rates scale approximately with the instantaneous luminosity, which is in turn expected to increase proportionally with the center-of-mass energy of the machines. The read-out speed requirements are therefore considerably more relaxed in the early low-energy stage (at $250 - 350$ GeV) than in the nominal 500 GeV stage and in the envisaged 1 TeV upgrade.

The DEPFET applies a rolling shutter read-out scheme, reading out two or four rows at any one time. The sequence involved in the read-out of one row in single-sampling mode is performed

[1] The ADC conversion factor is found to be approximately 10.2 LSB/μA in the DCDB [24], with a slight dependence on the read-out speed and the analog supply voltage. For the CURO system used to read out the thick sensor a conversion factor of 7.7 nA/LSB is used [30].

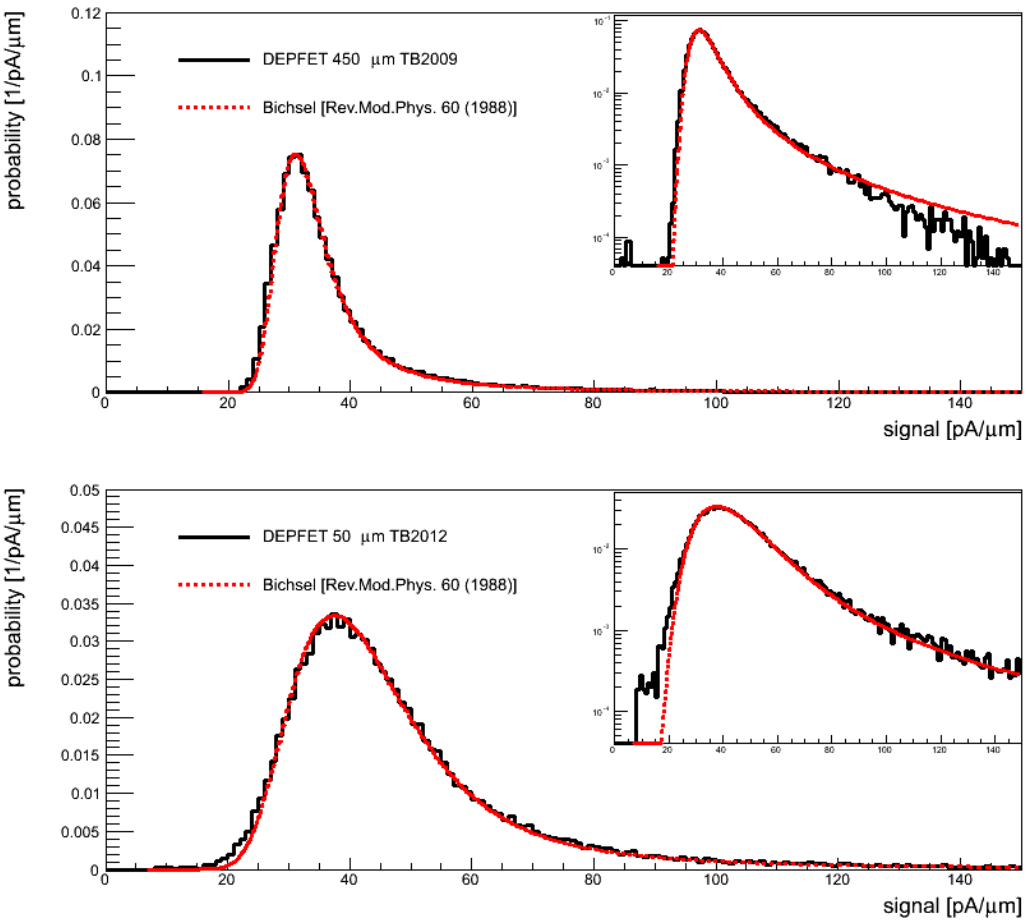

Figure 3: Signal distribution for a 450 μm thick DEPFET sensor (upper panel) and for a sensor thinned to 50 μm (lower panel). In both cases the measurement is expressed in pA per micron of active silicon. The measurements are compared to the prediction for the energy deposition in thin silicon layers of H. Bichsel [31]. The inset shows the same distributions on a logarithmic scale and with an extended axis range.

in less than 90 ns. With a column depth of 1025 pixels per half-ladder, and two rows sampled in parallel, this implies a read-out time for a complete frame of 40 μs, satisfying the stringent requirement for the innermost vertex detector layer. A factor two speed-up can be achieved by implementing four-fold multiplexing (i.e. reading out four rows of pixels instead of two). This requires an additional metal layer in the sensor.

CLIC envisages short bunch trains of order 300 bunches with a 0.5 ns spacing. Time stamping of single bunches in this environment requires devices with a read-out speed beyond the current state of the art, a challenge that the current DEPFET pixel detector concept cannot hope to address.

5. Power consumption & Cooling concept

The strict material budget of the LC vertex detector allows little room for cables to bring in power and the cooling system to remove the power dissipated in the tracker volume. At the ILC

colisions are delivered in a bunch train with a length of approximately 1 ms, after which the the machine is idle for 200 ms. Experiments plan to follow this 1/200 duty cycle by implenting a pulsed powering scheme, that strongly reduces the power consumption of the detectors during the idle period. Assuming a strong reduction of the average power consumption the vertex detector may be cooled by a forced flow of cool gas.

The DEPFET sensor with rolling shutter read-out is intrinsically well suited to this environment, as its power consumption scales with the number of pixels addressed in parallel (i.e. the number of read-out columns), rather than with the number of pixels. Only the pixels that are read out draw a current, the other pixels are switched off. For the layout sketched in Figure 1, and assuming 2-fold read-out, only 0.2% of pixels are active at any time during operation. The instantaneous power consumption of a half ladder is given by:

$$P = I_d \times V_{ds} \times n_{col} \times n_{\|} \sim 100\,\mu\mathrm{A} \times 5\,\mathrm{V} \times 1000 \times 2 = 1\mathrm{W}, \tag{5.1}$$

where I_d is the drain current, V_{ds} is the source-drain voltage, n_{col} is the number of columns in the sensor and $n_{\|}$ is the number of rows read out in parallel. Inserting measured values for the power consumption of the read-out chips the total instantaneous power required to operate a DEPFET vertex detector at the ILC is estimated at approximately 1 kW. The end-of-ladder where the four DCDs and four DHPs are located is the hottest point of the ladder, with a local power consumption of 6 W.

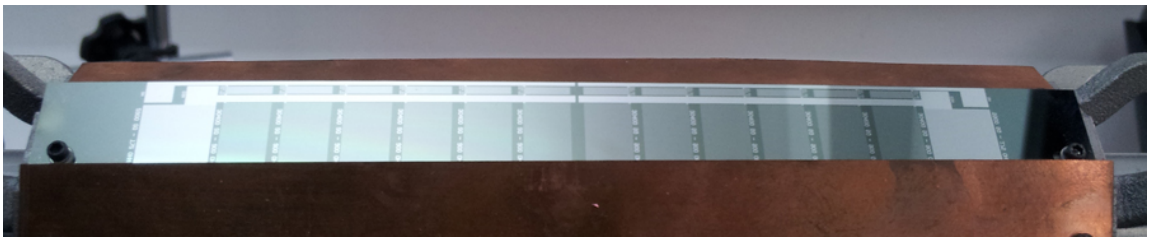

Figure 4: Photograph of a thermo-mechanical sample. The circuits that mimic the ASICs are clearly visible.

Cooling by a forced flow of cool gas is part of the Belle II cooling concept, where it is used to remove the heat generated in the central part of the sensor. Over the last years, a much better understanding of the potential of gas cooling was achieved through a combination of finite element model studies [34] and measurements [35]. Key measurements were performed on a sophisticated thermo-mechanical mock-up for a complete vertex detector in a realistic environment. The role of the sensors is taken by thermo-mechanical samples shown in Fig. 4. These are mechanically identical to DEPFET all-silicon ladders and have circuits in the relevant positions to mimic the power consumption of the ASICs and the sensor. Such *dummy* sensors with a barrel geometry have been extensively used to prove the principle of the DEPFET cooling concept [35]. With a newly developed power supply the measurements can be extended to include the impact of pulsed powering. A production run for *dummy* sensors with the petal geometry of the Forward Tracking Disks is ongoing at the time of writing.

6. Spatial resolution

The aim for the vertexing capabilities of the LC detectors is often summarized with the fol-

lowing requirement on the impact parameter resolution:

$$\Delta d_0 = 5[\mu\text{m}] \oplus \frac{10-15[\mu\text{m}]}{p[GeV]\sin^{3/2}\theta}. \tag{6.1}$$

The ILC experiments aim for a material term of 10 μm. This requirement is relaxed to 15 μm in the CLIC concepts as a consequence of the increased inner radius. This goal represents a improvement by a factor of six to ten with respect to most previous experiments. With the assumed inner radius of 15 mm this implies that the vertex detector must be built with a strict material budget of order 0.1% of a radiation length per layer. The DEPET material budget for the innermost layer presented in Fig. 2 represents a total of 0.15% of a radiation length.

Also the constant term in Eq. 6.1 is better by a factor of two to four than what was achieved at previous e^+e^- colliders and at the LHC. Simulation studies have shown that to achieve this goal each of the vertex detector layers must measure the position of charged particles with a resolution of approximately 3-5 μm.

Measurements on DEPFET prototypes yield a spatial resolution of close to 1 μm for thick DEPFET sensors with an ILC pixel design (thickness $\times$ pixel size of 450 $\times$ 20 $\times$ 20 μm^3) [36, 15, 16]. Thin Belle II design sensors with 50 $\times$ 50 $\times$ 75 μm^3 pixels yield a spatial resolution of 8 μm [29] for perpendicularly incident tracks. Both measurements can be reproduced by a detailed model of the DEPFET response, that we can therefore use with confidence to predict the spatial resolution of the ILC vertex detector design presented here. For a DEPFET device with 20 $\times$ 20 μm^2 pixels on a 50 μm thick sensor a spatial resolution of 3.5 μm is found for perpendicularly incident MIPs. The large magnetic field and frequent non-perpendicular incidence in the LC experiment lead to an average resolution that is significantly better than that.

7. Summary

In this Contribution I have reviewed the progress of DEPFET technology in the light of the requirements of a vertex detector for the experiments at a future e^+e^- collider at the energy frontier. Recent measurements on complete DEPFET active pixel detector prototypes and progress in the development and production of close-to-final-design read-out ASICs allow to estimate the performance with greater confidence. We expect a DEPFET-based vertex detector can achieve:

- a material budget of 0.15% radiation length/ladder, averaging over the acceptance
- a power budget compatible with cooling by a forced flow of cool gas
- a read-out speed of 80 ns to read out a single row of pixels and 40 μs to acquire a full frame
- a compfortable signal-to-noise ratio of approximately 40 with a 50μm thick sensor
- a spatial resolution of 3.5μm for perpendicularly incident MIPs

DEPFET technology thus confirms itself as a promising solution for a pixel detector in a future LC experiment.

References

[1] Howard Baer, Tim Barklow, Keisuke Fujii, Yuanning Gao, Andre Hoang, et al. The International Linear Collider Technical Design Report - Volume 2: Physics. 2013.

[2] Lucie Linssen, Akiya Miyamoto, Marcel Stanitzki, and Harry Weerts. Physics and Detectors at CLIC: CLIC Conceptual Design Report. 2012.

[3] M. Bicer, H. Duran Yildiz, I. Yildiz, G. Coignet, M. Delmastro, et al. First Look at the Physics Case of TLEP. 2013.

[4] F. Simon. Higgs Physics at future Linear Colliders - A Case for precise Vertexing. *These proceedings*, PoS(Vertex2013) 019.

[5] K. Agashe et al. Snowmass 2013 Top quark working group report. 2013.

[6] Y. Gershtein, M. Luty, M. Narain, L. T. Wang, D. Whiteson, et al. New Particles Working Group Report of the Snowmass 2013 Community Summer Study. 2013.

[7] J. Kemmer and G. Lutz. New detector concepts. *Nucl. Instrum. Meth.*, A253:365–377, 1987.

[8] G. Lutz et al. DEPFET-detectors: New developments. *Nucl. Instrum. Meth.*, A572:311–315, 2007.

[9] Rainer Helmut Richter et al. Design and technology of DEPFET pixel sensors for linear collider applications. *Nucl. Instrum. Meth.*, A511:250–256, 2003.

[10] P. Fischer et al. A DEPFET based pixel vertex detector for the detector at TESLA. LC-DET-2002-004.

[11] C. Lacasta. The DEPFET pixel detector for the Belle II experiment at SuperKEKB. *These proceedings*, PoS (Vertex2013) 005.

[12] The DEPFET collaboration. DEPFET active pixel detectors for a future linear e^+e^- collider. *IEEE Trans. Nucl. Sc.*, 60, 2013.

[13] Hans-Gunther Moser, Ladislav Andricek, Rainer Helmut Richter, and Gerhard Liemann. Thinned silicon detectors. *PoS*, VERTEX2007:013, 2007.

[14] L. Andricek, G. Lutz, Rainer Helmut Richter, and M. Reiche. Processing of ultra-thin silicon sensors for future e+ e- linear collider experiments. *IEEE Trans. Nucl. Sci.*, 51:1117–1120, 2004.

[15] Ladislav Andricek et al. Spatial resolution analysis of micron resolution silicon pixel detectors based on beam and laser tests. *Nucl. Instrum. Meth.*, A604:385–389, 2009.

[16] J. J. Velthuis et al. A DEPFET based beam telescope with submicron precision capability. *IEEE Trans. Nucl. Sci.*, 55:662–666, 2008.

[17] T. Abe et al. Belle II Technical Design Report. *KEK-REPORT-2010-1*, 2010.

[18] J. Knopf, P. Fischer, C. Kreidl, and I. Peric. A 256 channel 8-Bit current digitizer ASIC for the Belle-II PXD. *JINST*, 6:C01085, 2011.

[19] Ivan Peric, Tim Armbruster, Manuel Koch, Christian Kreidl, and Peter Fischer. DCD: The multi-channel current-mode ADC chip for the readout of DEPFET pixel detectors. *IEEE Trans.Nucl.Sci.*, 57:743–753, 2010.

[20] Ivan Peric et al. DCDB and SWITCHERB, the Readout ASICs for Belle II DEPFET Pixel Detector. *IEEE Nucl. Sci. Symposium Conference Record N31-5, pp. 1536-1539*, 2011.

[21] Jochen Knopf. *Development, Characterization and Operation of the DCDB, the Front-End Readout Chip for the Pixel Vertex Detector of the Future BELLE-II Experiment*. PhD thesis, Ruperto-Carola University of Heidelberg, 2009.

[22] L. Andricek, P. Kodys, C. Koffmane, J. Ninkovic, C. Oswald, et al. Advanced testing of the DEPFET minimatrix particle detector. *JINST*, 7:C01101, 2012.

[23] Stefan Rummel. *Investigation of DEPFET as Vertex Detector at ILC - Intrinsic properties, radiation hardness and alternative readout schemes*. PhD thesis, Technische Universitaet Muenchen, 2009.

[24] Manuel Koch. *Development of a Test Environment for the Characterization of the Current Digitizer Chip DCD2 and the DEPFET Pixel System for the Belle II Experiment at SuperKEKB*. PhD thesis, Ph.D. thesis Bonn University, CERN-THESIS-2011-084, 2011.

[25] L. Reuen et al. Performance of a DEPFET prototype module for the ILC vertex detector. *IEEE Trans. Nucl. Sci.*, 53:1719–1725, 2006.

[26] R. Kohrs et al. First test beam results on DEPFET pixels for the ILC. *Nucl. Instrum. Meth.*, A565:172–177, 2006.

[27] R. Kohrs et al. Development of a prototype module for a DEPFET pixel vertex detector for a linear collider. *IEEE Trans. Nucl. Sci.*, 52:1171–1175, 2005.

[28] M. Trimpl. *Design of a current based readout chip and development of a DEPFET pixel prototype system for the ILC vertex detector*. PhD thesis, Bonn University, Germany, 2005.

[29] MarÃğà Boronat Arévalo. *The spatial resolution of DEPFET active pixel detectors*. Master's thesis, Universitat de Valencia, Valencia, 2012.

[30] R. Kohrs. *Development and characterization of a DEPFET prototype system for the ILC vertex detector*. PhD thesis, Bonn University, Germany, 2008.

[31] Hans Bichsel. Straggling in thin silicon detectors. *Rev. Mod. Phys.*, 60(3):663–699, Jul 1988.

[32] ILD concept group. *The International Large Detector: Letter of Intent*. 2009. DESY 2009-87, Fermilab-Pub-09-682-E, KEK report 2009-6.

[33] H. Aihara, P. Burrows, and M. Oreglia, editors. *SiD Letter of Intent*. 2009. SLAC-R-944.

[34] C. Marinas. *DEPFET: A silicon pixel detector for future colliders. Fundamentals, characterization and performance.* PhD thesis, Ph.D. thesis Valencia University, CERN-THESIS-2011-101, 2011.

[35] Arantza Oyanguren. Air cooling for Vertex Detectors. *Proceedings of LCWS11*, 2012.

[36] L. Andricek, J. Caride, Z. Dolezal, Z. Drasal, S. Esch, et al. Intrinsic resolutions of DEPFET detector prototypes measured at beam tests. *Nucl.Instrum.Meth.*, A638:24–32, 2011.