PROCEEDINGS OF SCIENCE

Performance and operation experience of the ATLAS Semiconductor Tracker and Pixel Detector at the LHC

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The Pixel Detector and the Semiconductor Tracker are key elements of the tracking system in the ATLAS experiment at the CERN Large Hadron Collider. They provide precise measurements of charged particles trajectories in the region around the point where proton-proton collisions take place. The design and layout of both detectors are briefly described, before discussing their operations, data taking and performance over the course of LHC Run 1.

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1. Introduction

The ATLAS experiment [1] is a multipurpose detector taking data at the Large Hadron Collider (LHC) at CERN. It is designed to probe new physics phenomena at the energy frontier, by examining the products of proton-proton collisions taking place at the LHC. As most of the final states of collisions in the ATLAS experiment include charged particles, an excellent tracking system is essential. The ATLAS Inner Detector (ID) [2] is designed to measure the trajectories and momenta of charged particles within the pseudorapidity range $|\eta| < 2.5$, as well as both primary and secondary vertices. It comprises three independent but complementary subsystems, the innermost two are silicon detectors - the Pixel Detector [3], and the Semiconductor Tracker (SCT) [4], and the outer is a Transition Radiation Tracker(TRT) [5].

2. The Pixel Detector and the Semiconductor Tracker

The Pixel Detector is placed closest to the interaction point, and thus has the highest granularity. It consists of 1744 identical modules assembled on three concentric barrel layers and two endcaps with three disks each. In total there are about 80 million readout channels in the Pixel Detector. The intrinsic spatial resolution of individual Pixel Detector modules, is 10 μm in the $R-\phi$ plane and 115 μm in z (along beam axis). The Pixel modules are built of planar 250 μm thick $n-in-n$ Si sensors with 47232 pixels. The majority of sensors are identical and have a typical pixel size in $R-\phi \times z$ of 50×400 μm^2 , except for a fraction of long pixels with a size of 50×600 μm^2 located in the inter-chip regions. Each pixel module is read out by sixteen front-end chips (FE-I3 ASICs [6]) which are bump-bonded to the Si sensor. The front-end chip allows for pulse height measurements by means of a Time-over-Threshold (ToT) determination and performs zero suppression.An event building chip, the Module Controller Chip (MCC) [7], collects the data from the 16 readout chips. The data is then converted into an optical signal and sent via optical fibers to the off-detector electronics with a data transfer speed of 40 to 160 Mbit/s, depending on the layer. The MCC also distributes clock and control signals to the individual front-end chips.

The SCT is a microstrip silicon detector which surrounds the Pixel Detector layers. The SCT comprises four concentric cylindrical barrel layers, and nine circular endcap disks on each side, populated with 4088 silicon modules. It is designed to provide 8 measurements per track with a resolution of 16 μm in $R-\phi$ and 580 μm in z. A module is a basic unit in the SCT construction and readout. There are 2112 modules in the barrel, and 968 modules in each endcap. The barrel modules are rectangular and all identical in shape, while end cap modules can be of three different trapezoidal designs in order to fit efficiently to endcap disks. Each SCT module consists of two pairs of single-sided, 285 μm thick $p-in-n$ silicon sensors, each containing 768 AC-coupled readouts strips with 80 μm pitch on barrel modules and with a variable pitch averaging to 80 μm on the end cap modules. The two sensors are glued back-to-back around a central thermal pyrolitic graphite base-board and are rotated with respect to one another by a 40 mrad stereo angle to give the required space-point resolution. All the barrel modules and most of the end cap sensors are supplied by Hamamatsu Photonics [8], and $\sim$25% of the endcap sensors is supplied by CiS [9]. Each SCT module is equipped with 12 radiation-hard front end ABCD3TA chips [10] (henceforth referred to as ABCD), designed to read out signals from 128 strips. During operations, a bias

voltage is applied across the silicon, such that the holes produced by a charged particle traversing the sensor are collected at one or more of the strips. The resulting signals are amplified, shaped and discriminated to provide a binary readout that is latched to the 40 MHz clock. A hit is registered if the pulse height in a channel exceeds a preset threshold at the time of the clock signal.

In order to minimize the effects of radiation damage, both the Pixel Detector and the SCT are operated at a low temperature (-5 to -13 $^{\circ}C$ for Pixel and -7 $^{\circ}C$ to +4.5 $^{\circ}C$ for SCT). An evaporative cooling system with C_3F_3 as the coolant is used to keep silicon detectors at the optimal temperature.

3. ATLAS data taking

Since the LHC start in 2009, ATLAS has recorded an integrated luminosity of more than 25 fb^{-1}. In 2012 the center-of-mass energy was increased from 7 TeV to 8 TeV and the LHC luminosity was increased significantly, with a peak instantaneous luminosity reaching $\sim 8 \times 10^{33} \mathrm{cm}^{-2}\mathrm{s}^{-1}$.

A high instantaneous luminosity at the LHC is the biggest challenge for tracking and vertexing detectors, as they are particularly sensitive to the increase in particle multiplicity. In 2012 the mean number of inelastic proton-proton interactions (pp) per bunch crossing exceeded envisaged value of 23, and was over 30 for most of 2012. With higher particle multiplicity, the data taking can be disturbed by increasing number of readout chip errors caused by Single Event Upsets (SEUs), where a charged particle passes through on-detector electronics and changes a value stored in a memory cell. Despite these challenges, both Pixel Detector and SCT, performed very well throughout all data taking. For almost all operation periods, 99.3% of SCT and 95% of Pixel Detector were operational. The luminosity weighted relative fraction of good quality data delivered during 2012 stable beams in pp collisions by the Pixel Detector and SCT subsystems was 99.9% and 99.4% respectively [11]. Such an excellent data taking performance was possible thanks to the reliable and robust Data Acquisition System (DAQ). During operations, several enhancements were introduced into the DAQ in order to avoid potential sources of inefficiency. The SCT introduced online monitoring of chip errors in the data and the automatic reconfiguration of the modules with errors. In addition, an automatic global reconfiguration of all SCT module chips every 30 minutes was implemented, as a precaution against deterioration in chip configurations as a result of SEUs [12]. The Pixel Detector introduced special module auto-recovery procedures to detect the modules stuck in a permanent error state due to SEUs and reset them. These procedures minimized the number of module de-synchronisation errors as shown in figure 1 and reduced the average time it takes for a module in error mode to get inserted into data taking again from $\mathcal{O}$(s) to $\mathcal{O}$(ms).

The main component in the DAQ is the Readout Driver Board (ROD), which provides the front-end data flow, data processing and control of the detector modules. If any ROD experiences an error condition, it will exert a BUSY signal to stop the ATLAS data taking. From the beginning of data taking, each subsystem implemented an automatic removal of a busy ROD from the readout, thereby enabling to continue data taking while the cause of the BUSY was corrected. Automatic re-integration of a recovered ROD was also implemented.

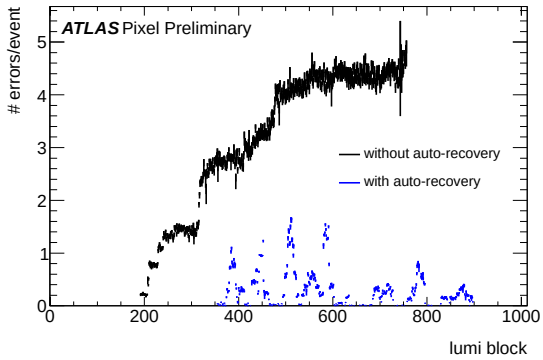

Figure 1: The average number of modules with readout errors per event in the innermost pixel layer (consisting of 286 modules), as a function of the time within a run expressed in luminosity block units (one luminosity block corresponds approximately to one minute of data-taking) [14].

4. Performance

4.1 SCT

In order to maintain a good tracking efficiency, the SCT input noise should be kept low. There are different methods of measuring the input equivalent noise charge (ENC, in units of number of electrons). It can be measured during analogue calibration tests in dedicated calibration runs, or during data-taking with events recorded while empty bunches pass through ATLAS. Figure 2 shows the distributions of chip-averaged response-curve noises as of October 2010 (top) and December 2012 (bottom), for different types of modules. After three years of operations, the noise levels stayed nearly at the original value for barrel and end-cap outer modules, while they increased about 15% in the end-cap middle modules with CiS sensors and about 5% in inner modules both with Hamamatsu and CiS sensors [13]. Overall, almost all SCT chips satisfy the SCT requirement of less than 5×10^{-4} in the noise occupancy for both periods.

The intrinsic hit efficiency measures the probability of a hit being registered in an operational detector element when a charged particle traverses the sensitive part of the element. A high intrinsic hit efficiency together with a low non-operational detector fraction are essential to ensure good-quality tracking. Modules, or module sides, or chips that are known to have either transient or longer-term problems with the readout, are excluded from the efficiency measurement. The individual bad strips contribute to efficiency calculation. Figure 3 shows the hit efficiency for each layer of the SCT detector and the fraction of individual disabled strips in each layer. The variation in efficiency from layer to layer primarily results from differences in the proportion of isolated disabled strips in each layer. The fraction of such strips in each layer is also shown in 3, and a clear anti-correlation with efficiency is seen.

4.2 The Pixel Detector

A three-year long successful operation of the Pixel Detector was possible due to rigorous tuning, monitoring and calibration procedures. Figure 4 shows the measured threshold and noise values of all pixels in the detector, after a tuning for a target threshold of 3500 e^-. As shown on

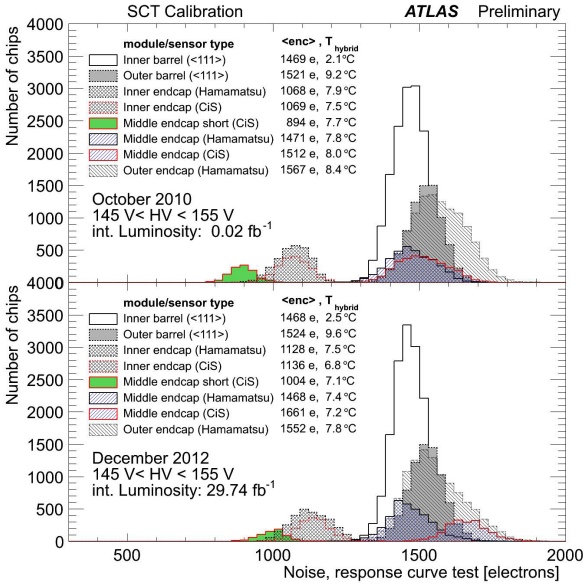

Figure 2: The distributions of chip-averaged response-curve noises as of October 2010 (top) and December 2012 (bottom)for various different types of modules [13].

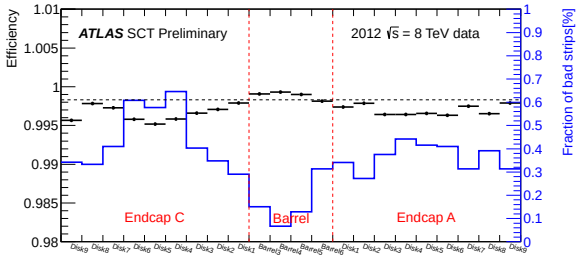

Figure 3: The mean intrinsic hit efficiency for each layer of the SCT measured in 8 TeV proton-proton collisions. The blue line and right-hand axis indicate the fraction of disabled strips in each layer [14]. The efficiency is measured using inner detector tracks with a transverse momentum of above 1 GeV and at least 6 SCT hits other than the one under consideration.

the left plot in figure 4, most pixels are well-centred around the target threshold value, the typical RMS of the threshold distribution after tuning is $\sim$ 40 e^-. The corresponding pixel noise in a normal pixel is typically about 170 electrons (see right plot in figure 4), and about 300 electrons for the class of the ganged pixels. This tuning results in a comfortable threshold to noise ratio of about 25 for all pixels apart from the ganged pixels, where it is about 10 [15]. Pixels exceeding a noise occupancy of 10^{-5} hits per bunch crossing (BC) in the dedicated noise data taking runs are masked for data taking already in the module configuration. At a threshold setting of 3500 e^- these pixels typically amount to 0.1% of all the total. On a run-by-run basis the remaining noisy pixels (typically 0.01% - 0.02% of all pixels) are determined in the first-pass reconstruction and are masked offline for the physics analysis. The noise occupancy after offline masking is $\sim 10^{-9}$ hits per pixel per BC.

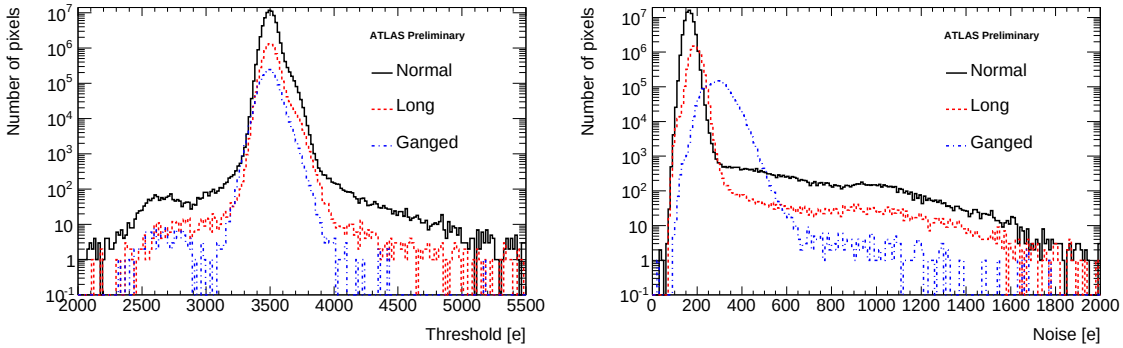

Figure 4: The threshold (left) and noise (right) for normal (black), ganged (blue) and long and interganged pixels (red). Ganged pixels are basically a combination of two pixels within one readout channel resulting thus in about twice the noise of a single "normal" pixel [15].

When a charge deposited in the pixel sensor is above the discriminator threshold, the front-end electronics stores the Time-over-Threshold (ToT) quantity, i.e. the time during which the pre-amplifier output is above threshold. ToT is measured in units of bunch crossings (units of 25 ns) and it has a nearly linear dependence on the charge released in the sensor. The time over threshold was calibrated so that a charge of 20ke produces a signal which stays over threshold for a time of 30 bunch crossings. After calibration and tuning the channel-to-channel variation amounts to less than 1 bunch crossing.The achieved ToT resolution is sufficient to determine the energy loss of the charged particle traversing silicon material with a resolution of 12%. This is sufficient to distinguish protons from kaons below 1 GeV in minimum bias events.

The Pixel Detector efficiency of finding a hit on the reconstructed track is shown in figure 5 for different pixel layers. The efficiency is $\sim$99% on most of the parts of the detector, slightly lower efficiency in the outermost disks (Disk3C and Disk3A) is due to few bad modules, identified already at the production stage.

5. Radiation damage

Some radiation damage effects in the SCT and Pixel Detector have become visible in 2011 and they are found to increase with the integrated luminosity. Significant increases in leakage currents have been observed in silicon detectors, as expected from the bulk damage due to the non-ionising energy loss of penetrating particles. Figure 6 shows by points the measured SCT leakage currents during 2010, 2011 and 2012 (left), and the evolution of high voltage current for the Pixel Detector (right). The predicted leakage currents by the Hamburg/Dortmund model [16] are shown by lines with colored bands indicating 1 sigma uncertainties. Results of the FLUKA simulation [17] of minimum bias events at 7 TeV pp collisions (with 5% up at 8 TeV) are used to convert the collision luminosity to 1 MeV neutron-equivalent fluence at each layer. The error of the FLUKA simulation is not included in the estimate of 1 sigma uncertainty. The SCT leakage current increase correlates closely with the delivered luminosity and temperature cycles. This dependence is well-understood and agrees with the leakage current predictions. For the Pixel Detector hight voltage currents, the model predictions underestimate the data, thus have been scaled up by 15% (layer 0) or 25% (layer

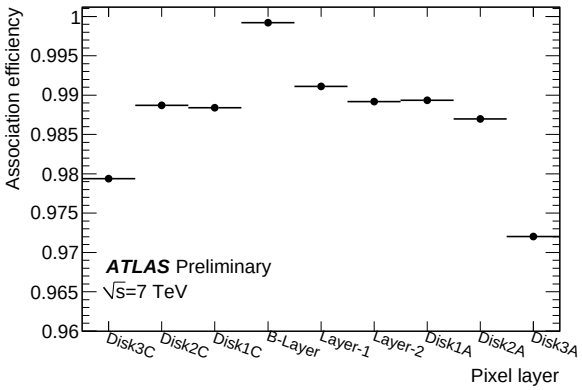

Figure 5: Efficiency for a track to have an associated hit when crossing the Pixel Detector layer. Dead modules are excluded from the efficiency computation, but other dead regions contribute to the inefficiency. 100% efficiency of the layer 0 (closest to the beam pipe) is due to the track selection, the lower efficiency for the most external disks is mainly due to inefficient regions on some modules. Error bars are smaller than marker sizes [14].

1 and 2), respectively. However given the different error sources of the modelling this is considered a good agreement.

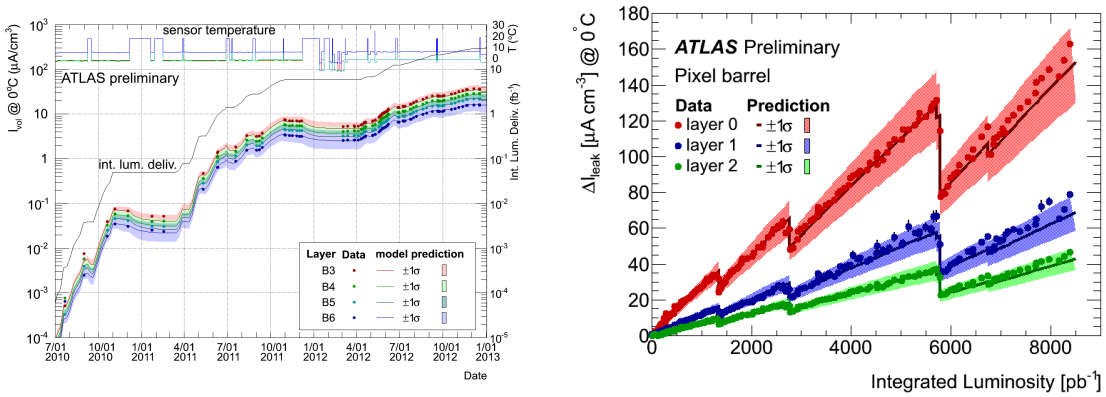

Figure 6: SCT barrel leakage currents during 2010, 2011 and 2012, showing correlations with a delivered luminosity and temperature, and compared to predictions from Monte Carlo (left)[13]. The averaged reverse-bias current for all Pixel modules in the different barrel layers as a function of the integrated luminosity (right). The model predictions underestimate the data, thus have been scaled up by 15% (layer 0) or 25% (layer 1 and 2), respectively [14].

In the longer-term, the crystal defect formation in the silicon bulk is expected to alter the effective doping concentration, producing type-inversion and ultimately an increase of the voltage required to fully deplete the sensor. The two innermost Pixel Detector layers, the layer 0 and layer 1, suffering most of the radiation, underwent the type inversion already in 2012, and the type inversion of layer 2 is foreseen shortly after the long shutdown. The decrease of the depletion voltage before the type inversion was clearly observed by measuring pixel cross-talk [18].

6. Combined performance

The measurements from the SCT and Pixel Detector, together with information from the TRT, are combined to provide excellent tracking and vertexing in ATLAS. Tracks above a given p_T threshold (nominally 0.4 GeV, however this value changes depending on the data) are reconstructed offline within the full acceptance range $|\eta| < 2.5$ of the Inner Detector, using multi-stage track identification algorithms [19]. The overall tracking performance can be described by the resolution of the transverse impact parameters d_0 of the tracks. The ID achieves a d_0 resolution of about 10 μm over the full acceptance range $|\eta| < 2.5$ for high momentum tracks.

The primary vertices are reconstructed using the iterative vertex finder algorithm [20]. Well reconstructed charged tracks are fitted to a common primary vertex. The beam spot is used as a three-dimensional constraint in the vertex finding algorithm and is routinely determined from the average vertex position over a short time period. The vertex position resolution in the collision data from 2012 is compared with Monte Carlo (MC) simulation in figure 7. There is a very good agreement at the level of 5% between data and simulation.

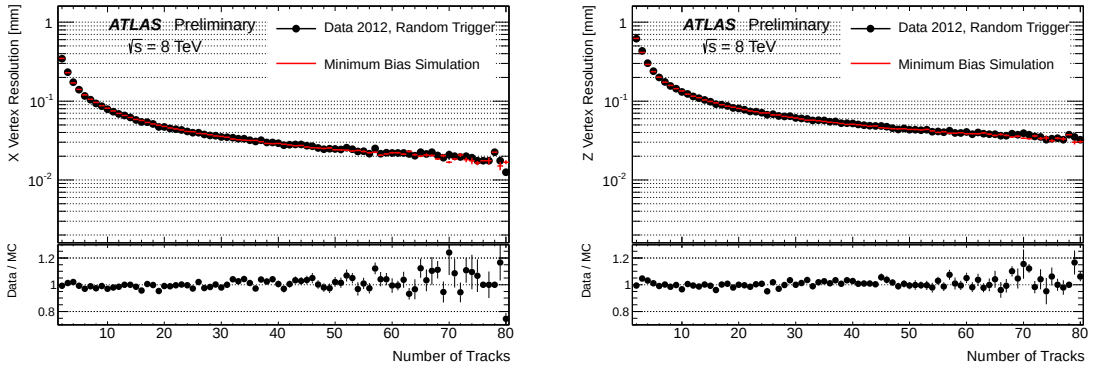

Figure 7: Vertex position resolution (with no beam constraint) in data (black) and MC (red). The resolution is shown for the transverse (left) and longitudinal (right) coordinate as a function of the number of tracks in the vertex fit. Data have been collected by a minimum bias trigger during a dedicated fill with an average number of interactions per bunch crossing of about 0.01 [21].

The vertices originating from the hadronic interactions of primary particles reconstructed in the data analysis, can be used to study the distribution of material in the Inner Detector volume. The reconstructed secondary vertices have a spatial resolution, approximately 0.2 – 1 mm, in both longitudinal and transverse directions [22]. This allows a precise radiography of the as-built tracking sub-systems and facilitates the comparison with the implementation of the detector geometry in Monte Carlo. This method confirmed that in general detector material description is in a very good agreement with MC. However, some discrepancies in the MC model have been discovered, the most important being that, in reality, the beam pipe is not centered around the (0,0) position. These features have been included in newer versions of the MC. Figure 8 shows the distribution of secondary vertices reconstructed in data. The beam pipe and sub-detector structures are visible. On the right a close-up picture for the Pixel module is presented, with hardware details clearly visible.

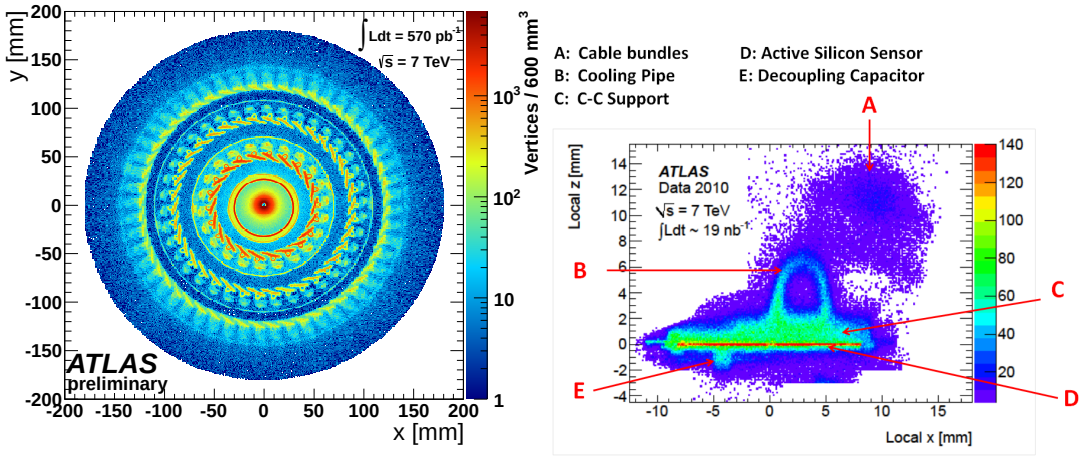

Figure 8: Plot of the (x, y) positions of reconstructed vertices with $|z|$ <300 mm and $x^2 + y^2 < 180$ mm. Vertices arising from hadronic interactions with the material in the beam pipe and the three barrel layers of the pixel detector are clearly visible (left). A "zoomed-in" view of z vs. x coordinates for the first layer of the Pixel Detector (right), various hardware features are visible [22].

7. Activities during the long shutdown

The LHC is currently stopped and undergoes a maintenance and upgrades. The machine is expected to restart in 2015 and collide bunches of protons with the center of mass energy of 14 TeV. It is not yet decided if the bunch spacing will be 25ns (design value) or 50ns (as it was so far), but either way, the detectors occupancy after the restart of the LHC will increase and rate of Level-1 trigger will rise up to 100kHz. Both the Pixel Detector and the SCT are expanding their DAQ systems to be able to handle larger volumes of data at a higher frequency after the LHC restart. In order to remove a critical bottleneck between the ROD and the next component downstream in the DAQ system, the ReadOut Subsystem (ROS), the SCT will install 38 additional RODs. Moreover, a new compression scheme will be used to encode hit clusters on the ROD. This means that the effective bandwidth into and out of the ROD will be similar.

In April 2013 the Pixel Detector was extracted from the ID and transported into the surface clean room for repairs and installation of the New Service Quarter Panels (nSQP). Most of the 88 pixel module failures were identified as damages on services due to the thermal cycling and have been repaired. In the new service panel installation the optical converters for data transmission are located 6.6 m from the collision point, thus their maintenance will be possible every year during short technical stops. The nSQP will also improve the data readout bandwidth of the pixel layer-1 to 160 Mbit/s, by doubling the number of optical fibers. Furthermore, a fourth layer of pixel detectors, the Insertable B-Layer (IBL),will be installed at the radius of 33 mm from the interaction point.

8. Summary

The Pixel Detector and the Semiconductor Tracker have performed very well since first collisions at LHC in 2009 till the beginning of the long shutdown in March 2013. Remarkably, 99% of

SCT detector and 95% of Pixel Detector was fully operational throughout three years of the LHC operations. The two silicon detectors have operated according to design requirements and together ensured that ATLAS has a reliable and precise charged-particle tracking system. Radiation damage is monitored and agrees with the expectations of the Hamburg/Dortmund model. The repairs and preparations for the LHC Run 2 are ongoing. The DAQ systems for both SCT and Pixel Detector are being prepared for higher luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$ expected in 2015.

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