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Overview of the ATLAS Insertable B-Layer (IBL) Project

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The upgrade of the ATLAS detector with a new layer of hybrid pixel detectors constitutes the first improvement of the tracking system for operation at the high luminosity LHC. The new sub-detector, called Insertable B-Layer (IBL), is currently under construction and will be installed between the existing pixel detector and a new beam pipe of smaller diameter. The increased radiation, pixel occupancy as well as the more stringent material budget and space requirements demanded the development of several new technologies for the IBL.
A novel ~ 4 cm^2 Front-End chip (FE-I4) in 130 nm CMOS technology, able to cope with 250 MRad total ionizing dose, was designed. To reduce the material budget the Front-Ends are thinned down to 150 μm and mechanical support structures, made of new composite materials with integrated CO_2 based cooling tubes, are deployed. Two different slim edge sensor technologies are used for the IBL: planar n$^+$-in-n sensors and, for the first time, innovative 3D sensors.
After a short overview of the IBL project the current status of the IBL production is presented with a focus on the quality assurance at wafer, module and stave levels. Particular emphasis is put on the results of the FE-I4 wafer probing that has been successfully completed. Final results including the yield and distributions of calibration values and important chip parameters are shown for 2580 Front-Ends tested.

11th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors
3-5 July 2013
Auditorium Cassa di Risparmio di Firenze, via Folco Portinari 5, Florence, Italy

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PoS(RD13)012

1. Motivation

The current ATLAS pixel detector consists of three barrel layers of hybrid pixel detectors and three forward and backward discs [1]. It provides high-resolution track points and is important for the identification of delayed particle decays via primary and secondary vertex reconstruction. Within the next few years of operation the expected particle fluence will exceed the design values for the pixel detector of 50 MRad ionizing and 10^{15} N_{eq}/cm^2 non-ionizing dose. The actual inner pixel layer (B-Layer) will be affected the most by the radiation. To counteract potential loss in the track reconstruction a new Insertable B-Layer (IBL) is being built. It will be inserted into the existing pixel detector as an additional barrel layer on a beam pipe of smaller diameter during 2014. The additional layer that is even closer to the interaction point increases the precision of the impact parameter reconstruction and reduces the ghost track probability induced by high pile-up events and can therefore enhance the vertex reconstruction and the B-tagging performance. The reduction of the radius of the innermost layer from 5 cm to 3 cm demands high radiation tolerance. During the IBL lifetime an integrated luminosity of 550 fb^{-1} will be collected leading to a total design fluence of 250 MRad ionizing and $5 \cdot 10^{15}$ N_{eq}/cm^2 non-ionizing dose (including safety factors) [2].

2. Layout

The IBL consists of 14 axial staves mounted onto support rings that are directly fastened to a new beryllium beam pipe of 2.5 cm radius. The staves are tilted by 14° in r-phi with 20% stave-to-stave overlap but no overlap in z-direction due to space constraints (Fig. 1). The support structure houses a titanium CO_2 evaporative cooling tube and is made of a carbon-fiber lamination filled

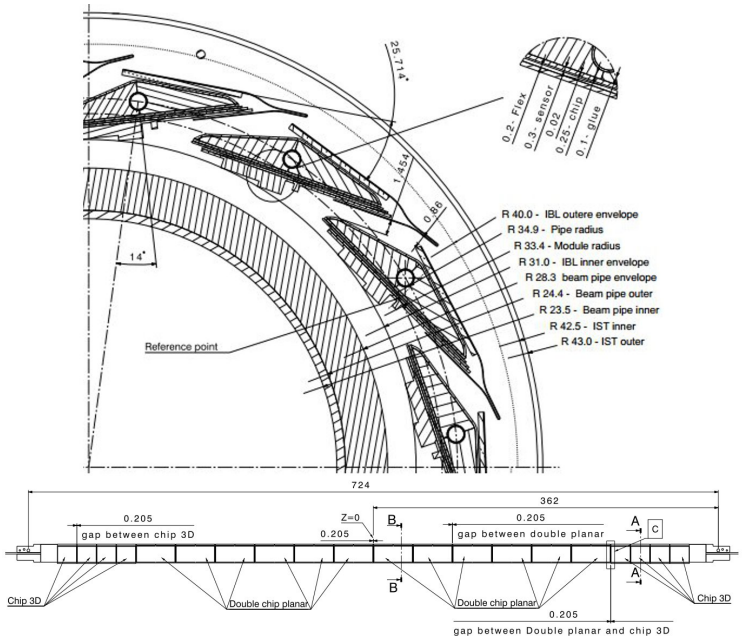


Figure 1: One quadrant cross-section of the IBL (top) and the top view of one stave (bottom). All dimensions are given in mm [2].

with low density carbon foam. This allows the reduction of the total radiation length down to only 60% of the present B-Layer and 1.54% X_0 at a pseudorapidity $\eta = 0$. Each stave contains 20 modules (Fig. 11), 8 single chip modules on either ends with 3D sensors and, 12 double-chip modules with planar sensors covering the central region. Four single chip or two double chip modules form one power group sharing the same high voltage and low voltage power lines. During stave production the modules are connected via wire bonds to a multi layer stave flex located at the stave back side (Fig. 1), containing power, data acquisition, and configuration lines.

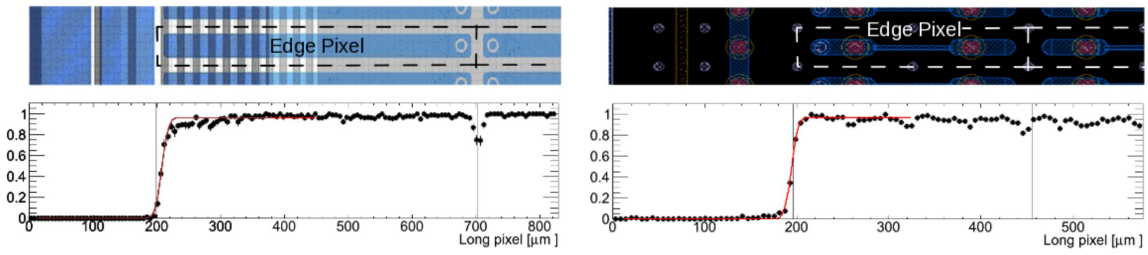
3. Sensors

Main requirements for the IBL sensors are slim inactive edges (< 250 μm), to be operational up to $5 \cdot 10^{15} \mathrm{N_{eq}/cm^2}$ NIEL, a maximum bias voltage of 1000 V and a power dissipation < 200 mW/cm^2 at -15° C working temperature. Two silicon sensor technologies with different electrode configurations have been qualified for IBL: planar n$^+$-in n and n-in-p 3D sensors. The properties of the two IBL sensors are listed in (Tab. 1).

Sensor technology	Planar n$^+$-in n	3D n-in-p
Electrode layout	Planar n$^+$-pixel and p backside	n and p-type columns
Thickness	200 μm	230 μm
Electrode distance	200 μm (= thickness)	67 μm
Operation voltage, begin/end of lifetime	60/1000 V	20/180 V
Manufacturer	CiS[1]	CNM/FBK
Tile size	18.59 mm x 41.32 mm	18.75 mm x 20.45 mm

Table 1: The properties of the two sensor technologies used in the IBL

The planar design is derived from a similar design employed in the current ATLAS pixel detector and constitutes a mature technology regarding the manufacturing yield and cost. The major advancement is the slim inactive edge (< 200 μm) achieved by shifting the back-side guard rings underneath the opposing edge pixels and by reducing the number of guard rings. The edge pixel layout and the measured efficiencies for the two IBL sensor technologies after high irradiation can be seen in figure 2.



(a) (b)

Figure 2: Edge pixel layout and edge efficiency of irradiated planar with $4 \cdot 10^{15}$ $\mathrm{N_{eq}/cm^2}$ (a) and 3D CNM sensors with $5 \cdot 10^{15}$ $\mathrm{N_{eq}/cm^2}$ (b) [4].

[1] CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Erfurt, Germany

The 3D sensors, on the contrary, have their first application in high energy physics. The main difference to the planar design is their electrode geometry. Instead of electrodes situated on the detector surface, they are etched into the sensor bulk as columns of 10 mm radius by double sided Deep Reactive Ion Etching (DRIE). The distances between the electrodes can be made shorter than the sensor thickness (IBL design: 67 μm) leading to a much lower depletion voltage. The reduced drift distance of the charge carriers also decreases the charge collection time and therefore the charge trapping probability making the 3D concept very radiation hard [3]. Two different 3D designs from two different manufacturers (CNM[2]/FBK[3]) are used for the IBL. In the CNM design, the columns are 210 μm long and isolated via p-stop/p-spray implantations on the n^+/p^+ side whereas the FBK design has electrodes that fully pass through the sensor bulk with p-spray isolation on both sides (Fig 3). In both designs each pixel has two n-readout electrodes and six

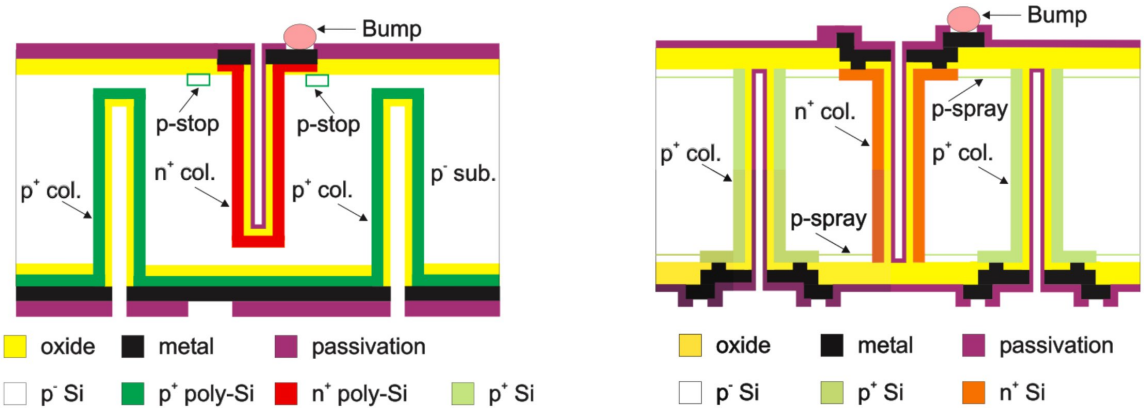


Figure 3: 3D sensor design from CNM (a) and FBK (b) [4].

p-type biasing electrodes shared with neighboring cells. A comprehensive overview showing the different sensor characteristics and test beam results of highly irradiated devices can be found in [4]. All IBL sensors have the same granularity of 250x50 μm^2 pixels (excluding the edge pixels) organized in 80x336 arrays. 75% of the IBL sensor surface will consist of planar sensors, where one sensor tile is bump bonded to two FEs (double chip module). The remaining 25% are made of 3D sensors with tiles that are half the size of the planar tiles due to yield limitations. Each 3D sensor is read out by one FE, forming a single chip module.

4. Front-End I4

The FE-I4 integrated circuit is designed in a 130 nm CMOS process offered by IBM. With a dimension of 20.2 x 18.8 mm^2 and an active area of 20.2 x 16.8 mm^2 (89%) it is currently the largest chip produced for high energy physics. To cope with the high pixel occupancy the readout architecture of the FE-I4 is very different compared to its predecessor the FE-I3. The hits are stored in local pixel buffers organized in 4 pixel digital regions (PDR). These localized buffers exploit the

[2]Centro Nacional de Microelectronica (CNM), Barcelona, Spain.
[3]Fondazione Brune Kessler (FBK), Trento, Italy.

fact that real hits usually come in geographical proximity and avoid unnecessary copying of the hit information to the periphery of un-triggered hits. This is the main source for the hit inefficiency of the FE-I3 design at IBL conditions [5]. The pixel matrix of the FE-I4 has 26880 pixels of 50 μm x 250 μm sizes organized in 336 rows and 80 columns.

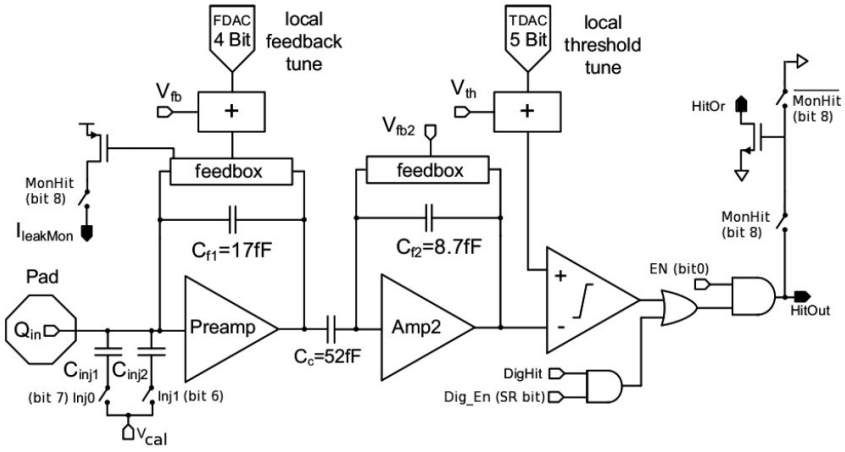


Figure 4: The analog pixel cell of the FE-I4 [6].

Each pixel of the FE-I4 has a two staged AC coupled charge sensitive amplifier with adjustable shaping time for the first stage and an individually adjustable threshold for the discriminator that follows the second stage (Fig. 4). The charge determination and time stamping is done via the time over threshold (TOT) technique with 4-bit resolution. One TOT is given in counts of an externally supplied clock, nominally 40 MHz. For the tuning and testing of the FE an internal charge injection circuit (Pulser DAC) can be used that distributes a voltage step (V_{cal}, Fig. 4) to selectable injection capacitors present in each pixel. The data output during detector operation is an 8b/10b encoded LVDS signal with 160 Mb/s.

For the IBL production the 2nd full scale version of the FE-I4 is used, called FE-I4B. Only minor changes were needed to its predecessor the FE-I4A that already fulfilled most of the IBL requirements, like the radiation hardness (> 250 MRad) and the power consumption (< 2 mW/ mm^2) [4]. The changes are mainly related to the homogeneity of the pixel matrix, the implementation of an internal power management, the improvement of the internal charge injection circuit and, the tuning of biasing DAC and counter ranges [6]. The FE-I4B has two stand-alone low dropout voltage regulators (LDO) that are used during IBL operation to generate the analog and digital supply voltage [7]. The reference voltage input of each LDO has to be half the value of the desired output voltage and can be either connected to an internal tunable voltage reference or a voltage band gap circuit. The tunable voltage reference uses the master current reference of the FE-I4B (nominally 2 μA) from which all internal DACs and biases are fed. Since this reference current itself relies on the output of the analog LDO a power up circuit was implemented. In order to maximize the probability of a successful startup at low temperatures (-40°C) and to ensure an operation voltage of < 1.6 V after high irradiation, a powering scheme was chosen where the voltage reference of the LDO powering the analog part is fed by both voltage references and the digital LDO by the tunable reference only. Detailed information and measurements of the IBL low voltage powering scheme can be found in [8].

5. FE-I4B wafer testing

The FE-I4B is produced on a 200 mm wafer with 60 chips. All 43 wafers (2580 chips) for the IBL have been tested and selected results are presented here. During the test of each wafer the FEs are probed sequentially by contacting 108 FE pads with a needle card (Fig. 5). The measurement time is one hour per chip and 2.5 days per wafer. The tests can be divided into three parts: Pixel array tests where the analog and digital functionality of each pixel is tested, global chip tests where global chip parameters are investigated and chip calibrations [Tab. 2]. The chip calibrations require to contact dedicated pads of the FE and are therefore only possible at wafer level. The deduced calibration values are crucial for the detector operation and the measurements cannot be repeated at a later stage of the IBL production.

Pixel array tests	Global Front-End tests	Front-End Calibrations
Analog tests with internal charge injection circuit (Analog scan with different injection capacitances, Threshold scan for pixel noise and threshold, Cross Talk scan)	Current consumption (at power up, after configuration, at high trigger rate)	Reference current tuning
Test of the digital hit processing periphery (Digital scan, Hit buffer test, Latency counter test, Hit Or test)	Global register tests	Voltage references measurements
Configurability of the pixels (Pixel register tests, Masking capability)	Event size limitation test	Internal charge injection circuit (Pulser DAC transfer function, Injection capacitance measurement)
	Service record counter readout	Serial number burning [4]
	Scan chain tests of three main logic blocks (CMD, DOB, ECL)	

Table 2: Complete list of all tests done during FE-I4B wafer probing for IBL.

More than 18000 values are collected for each wafer demanding a fully automated analysis. Therefore a custom software[5] was designed to determine the chip states autonomously by applying a sophisticated cut scheme on pixel, column and Front-End levels (Fig. 6). The cut values are defined via the study of distribution plots of the first 10 wafers and by the knowledge already gained from FE-I4A wafer probing. At the end of the analysis each FE is classified with a color: red, yellow, green, blue. Red Front-Ends show an extreme current consumption and cannot be configured, yellow FEs are partially working and can be used for R&D purposes, blue FEs have results that the software cannot judge automatically and green FEs pass all tests and are selected for IBL. At the beginning of each FE test the reference current is set, since it has a big impact on the power consumption and the overall chip performance. It can be tuned to the design value of 2 μA with small deviation (<25 μA RMS, Fig. 7 (a)). After tuning of the reference current the chip is configured

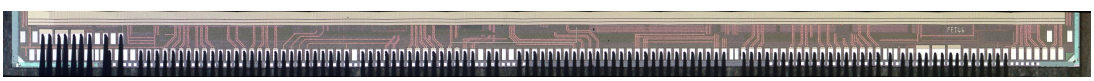


Figure 5: Probe needles contacting 108 FE-I4B pads during IBL wafer probing.

[4] 15-bit: chip number (bit 1-6) + wafer number (bit 7-15)

[5] WaferAnalysis, http://icwiki.physik.uni-bonn.de/twiki/bin/view/Systems/UsbPix#WaferAnalysis

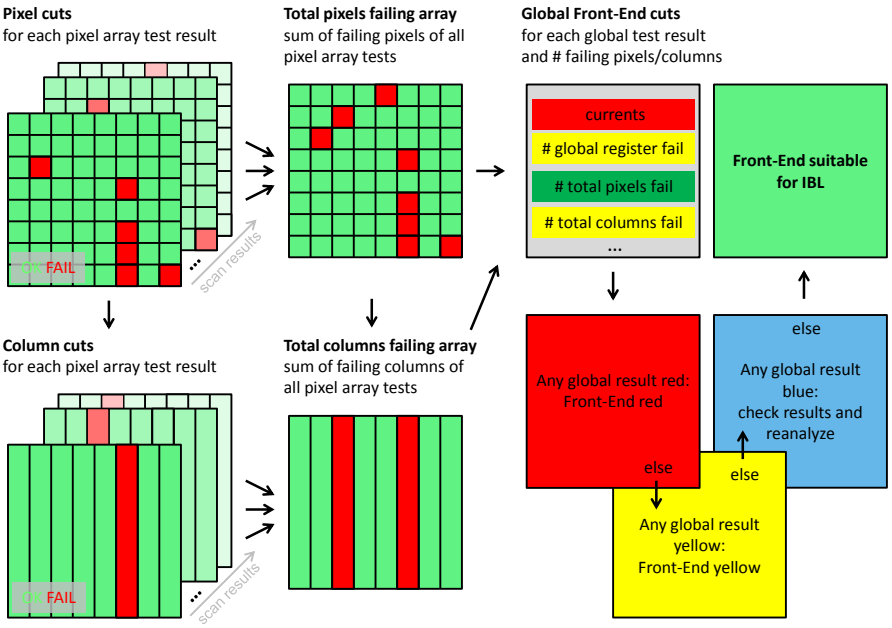
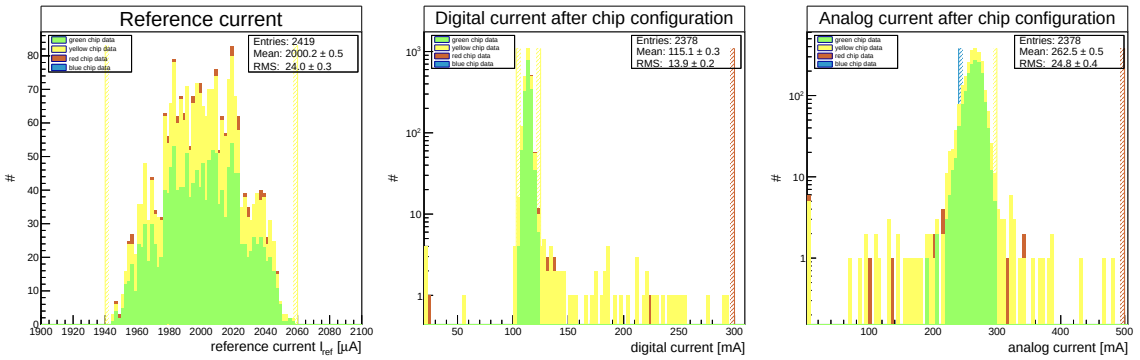


Figure 6: Cut scheme used for FE-I4B IBL wafer probing. Black arrows indicate the cut flow. Left: Cuts are applied on pixel level for each pixel array test, defining failing pixels. If more than a certain number of pixels in one column fail the column is marked as fail. Middle: All failing pixels/columns of all pixel array tests are summed up to avoid double counting. Right: Global cuts on global results and the total number of failing pixels/columns define the final chip state. Only if no result is marked red, yellow or blue the Front-End is green and therefore accepted for IBL.

with the standard configuration (listed in [6]) and the current consumption of the digital and analog part is measured. The distribution of these values and the corresponding cuts depicted as vertical lines are plotted in figure 7 (b), (c). All green FEs have a digital current consumption in a narrow



(a) (b) (c)

Figure 7: Current distributions of the FE-I4Bs tested for IBL. The colors of the histograms show the final chip state and the vertical lines the cut values. Figure (a) depicts the reference current distribution after tuning to 2 μA. Figures (b) and (c) show the current drawn from the digital/analog part with 1.5 V/1.2 V supply voltage after configuration with standard settings (listed in [6]).

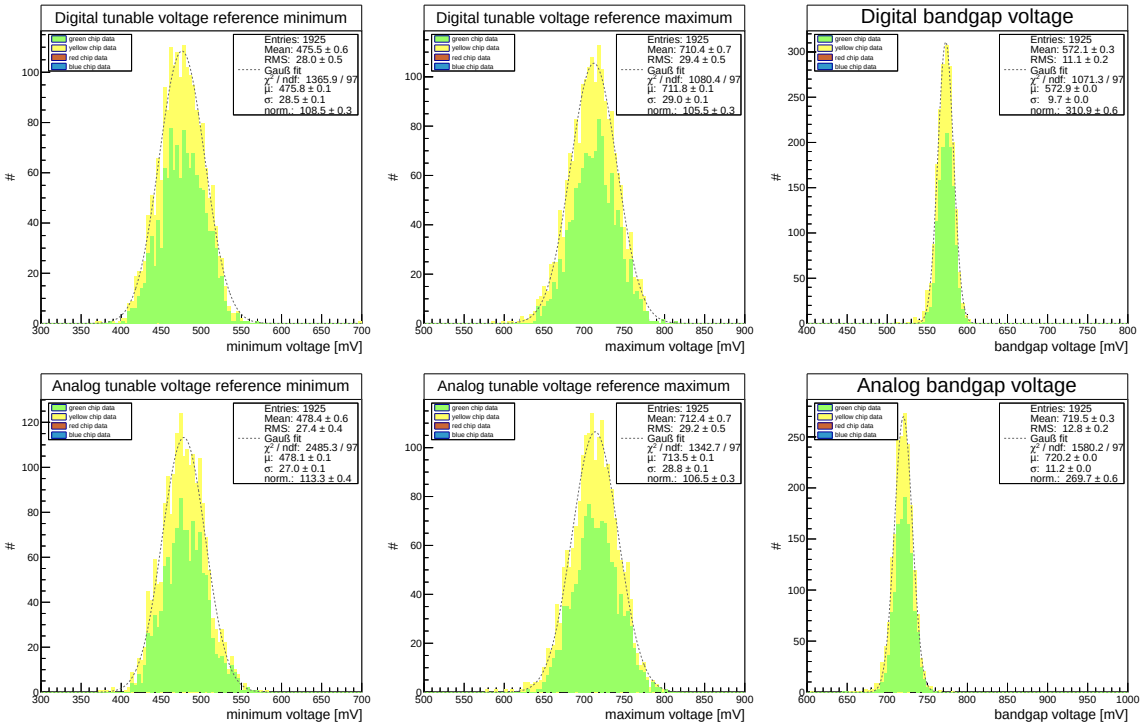


Figure 8: Results of the reference voltage measurements for the digital (top) and analog (bottom) regulators. Left/middle: minimum/maximum archievable voltages of the tunable voltage references. Right: distributions of the bandgap voltage references. The corrected reference voltages were determined on 37 IBL wafers only.

range between 105-125 mA. The analog current distribution is rather broad (200-300 mA) since the quality of the needle contact can reduce the analog current drawn up to 80 mA. Therefore no FE is disqualified if only the analog current is too low.

The voltage references for the two on chip regulators were also measured on the wafer (Fig. 8). No cuts were applied to these values due to an unsettled power scheme at the time of wafer probing. In

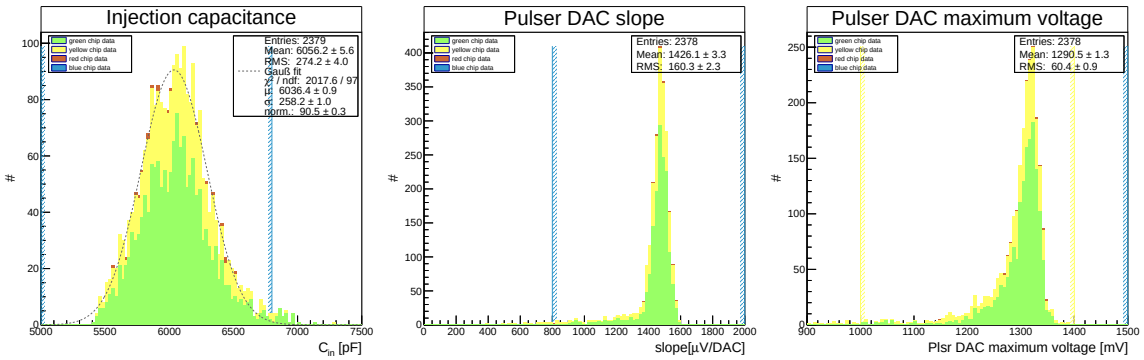


Figure 9: Calibration values for the internal charge injection. The left figure shows the distribution of the measured injection capacitance values and the middle and right figures the slope of a line fit to the PlsrDAC transfer function and the PlsrDAC maximum voltage.

addition it is difficult to measure voltages precisely on the wafer because of the resistances coming from needle contact leading to a voltage shift greater than 60 mV. To correct for the voltage shift all reference voltages are measured at three different current consumptions and a linear extrapolation to zero current is done. Nevertheless an offset in the order of few tens of mV can still be seen when comparing voltage measurements with the needle card and with wire bonded FEs. Taken this systematic error into account the digital and analog bandgap voltages with 572 ± 11 mV and 720 ± 13 mV are close to their design values of 600 mV and 750 mV. In contrast the maximum tunable voltage reference for the analog part (Fig. 8) is often much lower than 750 mV. Therefore the analog voltage used during detector operation was lowered from 1.5 V to 1.4 V.
Figure 9 shows the calibration values for the internal charge injection. The values of the injection capacitances are 6.1 ± 0.3 fF and in good agreement with the simulations. The slope of the linear PlsrDAC transfer function (1.5 ± 0.2 $\frac{\text{mV}}{\text{DAC}}$) and the archivable maximum voltage (1.43 ± 0.16 V) meet the expectations. However a small fraction ($< 3\%$, Fig. 10) of the Front-Ends do not reach the required maximum PlsrDAC voltage of 1 V, which was chosen to ensure the capability of time walk measurement on the stave.

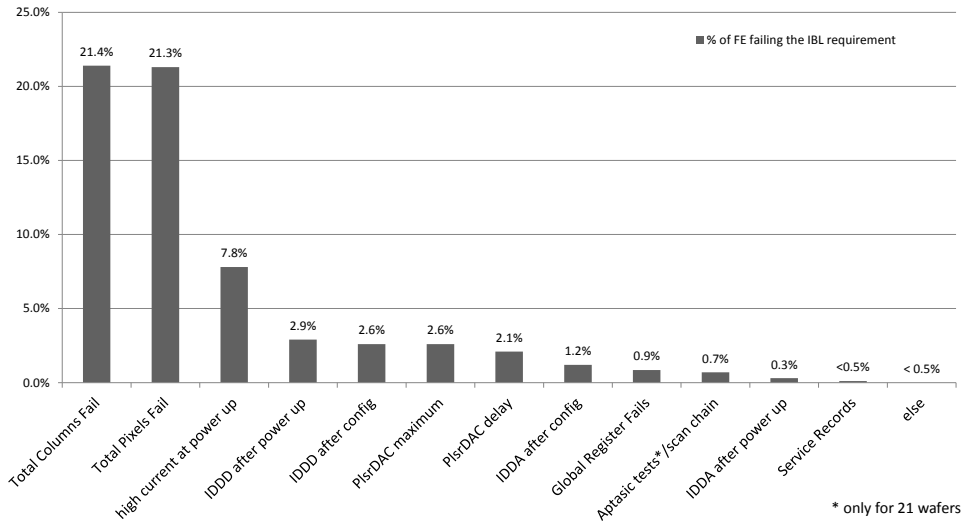


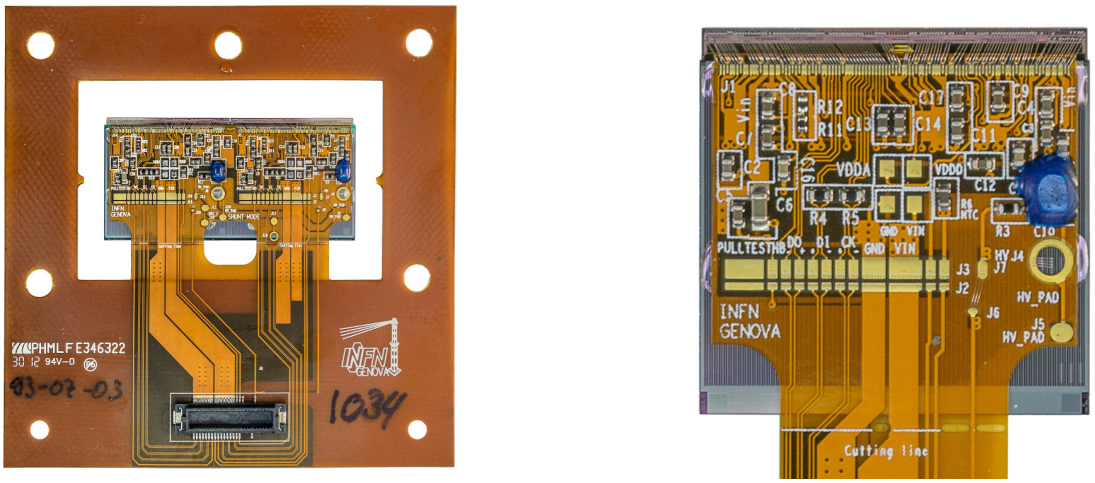
Figure 10: Most frequent test results that lead to the disqualification of the FE-I4B for IBL.

In total 61% of the tested chips qualify for IBL, 30.5% are marked yellow and 8.5% red. There is no correlation between the failure rate and the FE position on the wafer, besides two FEs that are produced very close to the wafer edge. The most frequent test result leading to a disqualification of the FE is the total number of failing pixels and columns (Fig. 10). The FE is only accepted if less than 0.2% (54 pixels) are failing with less than 20 pixels per column. Fig. 10 also shows the second most frequent failure mode, which is the current consumption (IDDA, IDDD, high current at power up). Additional IDDQ and Shmoo plot tests (bin 'Aptasic tests') have been carried out at an external company[6] for the first $\sim$ 20 wafers only, since the failure rate is very low ($< 0.5\%$).

[6] Aptasic SA, Boudry, Switzerland.

6. Module testing

After the qualification of suitable Front-Ends and sensors the FE is thinned down to 150 um and both parts are connected on a pixel basis via bump bonds [9]. A flex is glued onto the sensor and the flex pads are connected to the FE pads with wire bonds. The whole assembly is called module (Fig. 11).

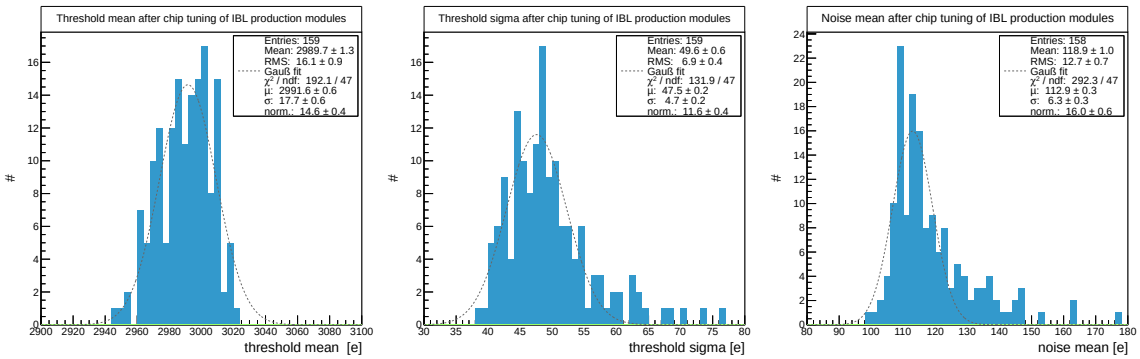


(a) (b)

Figure 11: Modules of the IBL. (a): double chip module with handling frame and module connector, (b) magnification of a single chip module with FBK 3D-sensor. VDDA/VDDD pads are used to sense the regulator output voltage.

During module testing the bump bond quality is checked with several tests before and after thermal cycling between -40° C and 40° C. There are two possible failure modes for the bump connection: open and shorted bumps. Open bumps are detected with a source scan and by the comparison of the pixel noise with and without sensor bias. The noise is different if the sensor pixel is connected due to the change of the input capacitance of the preamplifier. Shorted bumps are identified in a cross talk scan, where charge is injected into selected pixels and neighboring pixels are read out. A large fraction ($\sim 37\%$) of the first 195 modules tested showed too many open and shorted bumps. Therefore the bump bond process was changed to a flux free process leading to an increase of the module yield to a reasonable 80%.

During the module tests the FE is powered for the first time with the final powering scheme using the regulators. The output voltages of the regulators are sensed on special pads on the module flex (Fig. 11(b)) and are tuned to 1.2 V for the digital and 1.4 V for the analog part. Also the tuneability of the threshold is tested for the first time at module level and initial configurations for the detector operation are created. The distribution of the threshold mean and the threshold spread after chip tuning can be seen in Figure 12 together with the mean noise. The small spread of the threshold distribution (< 17 e offset, < 50 e sigma) illustrates sufficient tuning capabilities. The noise between $100 - 150$ e matches the the expectation and is a good indicator for a successful FE calibration. The distribution is not normally distributed, since the 3D sensors have a higher



(a) (b) (c)

Figure 12: Threshold and noise of 159 IBL production modules after FE tuning to 3000 e threshold. (a) and (b): mean threshold and dispersion determined by a Gauss fit, (c): arithmetic mean noise.

capacitance [10]. All results taken during module testing are analyzed with the same cut scheme used for FE-I4B wafer probing (Fig. 6). Modules are only accepted if the sensors have a reasonable break down voltage, the FE is working with the regulators and the number of broken pixels is less than 1%, i.e. 270 per chip. With the actual qualification rate the module testing will be finished in October 2013.

7. Stave testing

After the modules are selected for IBL they are glued onto the bare staves and sent to CERN. At CERN a test bench has been established to ensure the overall functionality of the assembled staves [11]. The staves are reviewed under clean room conditions and under controlled humidity at warm ($\sim 10^\circ$ C) and cold ($\sim -15^\circ$ C) temperatures. To mimic the detector operation conditions all modules are operated in parallel. The cooling is done with CO_2 evaporative cooling as it is done in the detector.

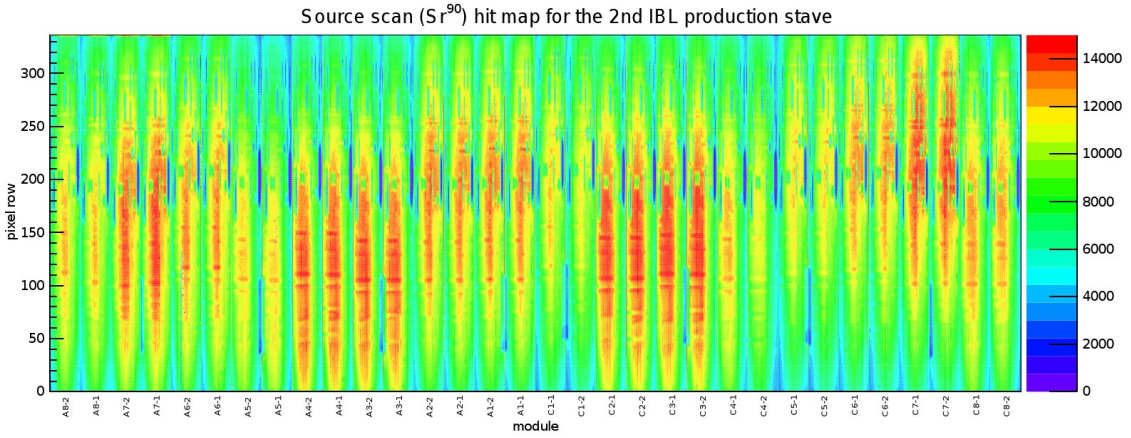


Figure 13: Hit map of a source scan with Sr^{90} of the 2nd production stave.

After the reception of a stave a visual inspection for transport damages is done and power up and communication tests are performed on every module. The communication tests include FE register tests and the recording of eye diagrams for data transmission. The sensors are checked with IV curves and the total number of bad pixels per stave is determined in different scans. Bad pixels are defined by their non-responsiveness to charge injection, noise occupancy and bump bond failures. Also different tunings for the whole stave are created with a threshold of 1500 e, 2000 e, 2500 e and 3000 e. To evaluate the overall detection performance beta, gamma-sources and cosmic rays are used. An example of a Sr^{90} source scan of the 2nd production stave showing a good response of all modules can be seen in Figure 13. The source was moved by a linear motor stage along the stave with a speed slow enough to hit every pixel with a high probability. The rate is altered by a different material budged from the flex between source and sensor. At the end of a stave test the bad pixels are summed up and taken as a measure to rank the stave. The best 14 staves out of presumably 17 staves built will be used for IBL. At the time of writing already 8 staves have been successfully qualified and the numbers of bad pixels with 1500 per stave ($< 0.2\%$) is remarkably low. The last stave is expected to be qualified in the last quarter of year 2013.

8. Conclusion

The IBL is the new fourth layer for the ATLAS pixel detector and currently under construction. New lightweight materials, novel radiation hard, slim edge sensor technologies and a new Front-End will be used in the new layer. The production of all detector components is already completed and the quality assurance for the FE-I4B is finished with a reasonable yield of 61%. The module production is expected to finish within fall 2013 and halfe of the needed staves qualified already with a small number of bad pixels ($< 0.2\%$). During the next year, 2014, the new layer will be inserted into the existing pixel detector.

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