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The phase-1 upgrade of the CMS silicon pixel detector

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For the CMS collaboration

The present CMS pixel detector will be replaced in the shutdown period 2016/17 by an upgraded version due to the following reasons: increased luminosity at reduced bunch spacing (from 7 x 10^{33} cm^{-2} s^{-1} at 50 ns bunch spacing to 2 x 10^{34} cm^{-2} s^{-1} at 25 ns bunch spacing) in the LHC, and radiation damage effects that will significantly degrade the present detector. The new upgraded detector will have higher tracking efficiency and lower mass with four barrel layer and three forward/backward disks to provide higher hit pixel coverage out to pseudorapidities of ±2.5. In this paper we will describe the new pixel detector focusing mostly on the barrel detector design, construction and expected performances.

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1. Introduction

The operation of the present pixel detector started in 2010 with LHC operating at a center of mass (CM) energy of 7 TeV. By the end of 2011, a data sample with integrated luminosity of 6 fb^{-1} was collected by CMS. At the beginning of 2012 CM energy was increased to 8 TeV and within December 2012 a total of 19 fb^{-1} integrated luminosity has been delivered, with instantaneous peak luminosities approaching 7 x 10^{33} $cm^{-2}s^{-1}$. The present pixel detector originally was designed for a luminosity of 1 x 10^{34} $cm^{-2}s^{-1}$ and a pileup (number of inelastic interaction per bunch crossing) of 25 in 25 ns bunch spacing. Since these beam parameters will be reached only after the long shutdown period ending in mid 2014 (with an additional increase in the center of mass energy up to the value of 13-14 TeV) and then peak luminosity will keep increasing until late 2016 when it will reach the value of 1.5 x 10^{34} $cm^{-2}s^{-1}$, the detector, that has worked very well so far, will remain operative until that date, afterwards the beam parameters will change again as shown in Fig.1. For that period an increase of peak luminosity reaching at least 2 x 10^{34} $cm^{-2}s^{-1}$ is foreseen, consequently pile-up will increase up to 50 if the bunch spacing will be kept at 25 ns, or to 100 if the bunch spacing will be brought to 50 ns. In this context the present pixel detector, as will be shown in the next session, will be unable to perform adequately and a new detector needs to be built before [1].

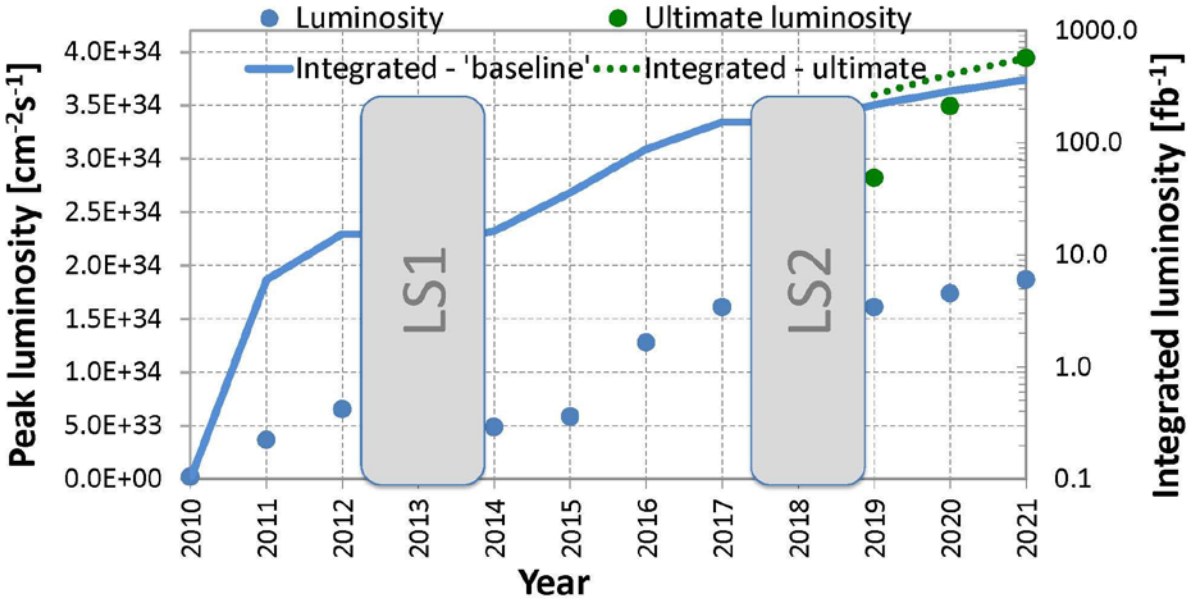

Fig.1 LHC luminosity foreseen in years 2010-2021. The continuous blue line shows the integrated luminosity reaching 500 fb^{-1} by the year 2023 the blue (and the green) dots shows the instant peak luminosity for 25 ns beam spacing reaching 2 x $10^{34}cm^{-2}s^{-1}$(or even 4 x $10^{34}cm^{-2}s^{-1}$) in 2021.

In addition to the data loss problem and fake rates induced by the increased luminosity also the issue of radiation damage will start to play a role in the necessity to build a new pixel tracker. Fig. 1 shows that in 2021 the integrated luminosity will reach the value of 500 fb^{-1}, simulations show that such a luminosity corresponds to about 3 x

10^{15} neq/cm^2 in the first layer of the pixel tracker (corresponding to 1 MGy of total ionizing dose), while layer 3 of the present pixel detector will receive about 6 x 10^{14} neq/cm^2; at these value of irradiation the charge collection efficiency of the pixel sensor is degraded as shown in Fig.2 [2]. In particular for layer 1 we expect a charge collection efficiency of about 25-35% the original value and for layer 3 this charge collection efficiency will be 50-60%. Also for this reason a detector replacement is mandatory before reaching 500 fb^{-1} of integrated luminosity.

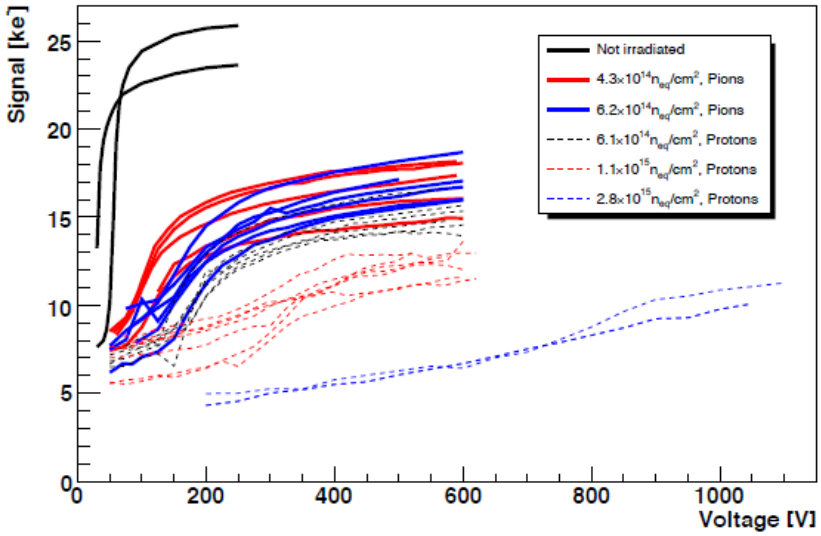

Fig.2 Charge collection of the present pixel silicon detector at various level of irradiation.

2. The design performances of the new pixel detector

In order to overcome the problems described in section 1 a new detector design is foreseen for installation in the shutdown period (winter 2016-2017) before long shutdown 2. Although some action will be performed to compensate the reduction in charge collection efficiency due to irradiation, the main problem to be solved is the reduction in overall tracking efficiency and the increase of the fake rate due to the increased peak luminosity. Detailed simulations have been performed to improve the present pixel detector and the main results will be shown in this section.

In this paper the tracking efficiency is defined as the ratio between the number of truth tracks (generated by event generator monte-carlo) matched by the reconstructed tracks and the total number of generated truth tracks; the fake rate is the ratio between: the number of reconstructed tracks NOT matching the truth tracks and the number of total reconstructed tracks.

The design geometry for the new detector compared with the previous detector is shown in Fig.3b. The new detector will have four layers of barrel pixel detector (BPIX) compared to 3 layers of the previous detector, and 3 layers per side as endcap pixel detectors (FPIX) compared to 2 layers of the previous detector. To reduce the overall material budget (shown in Fig.4) some design solution have been adopted and they will be described in the forthcoming section. The pixel geometry has been

unchanged compared to the previous detector, the silicon pixel sensor has overall lateral dimensions of 16.2 x 64.8 mm^2 thickness of 285 ± 5 μm and pixel size 100 x 150 μm^2 (for a total of 66560 pixels/detector) [3].

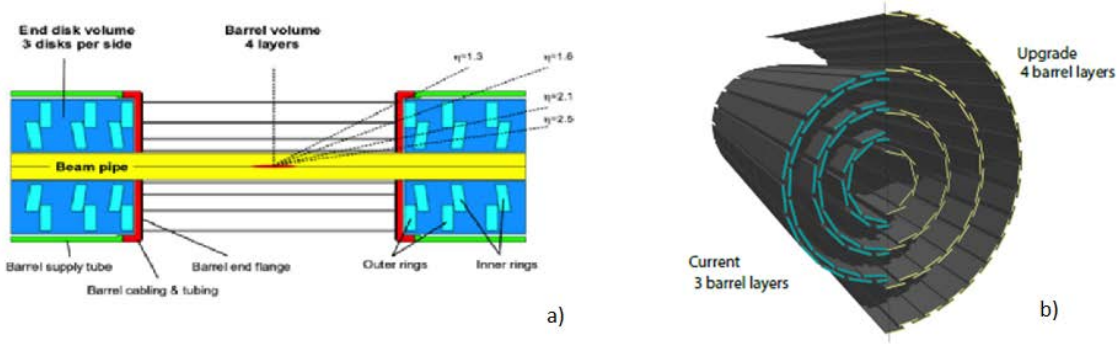

Fig.3 Structure of the new pixel detector. a) the layer structure of the overall detector that includes 4 barrel layers and 3 endcap layers of sensors. b) comparison between the current structure of BPIX versus the upgraded structure.

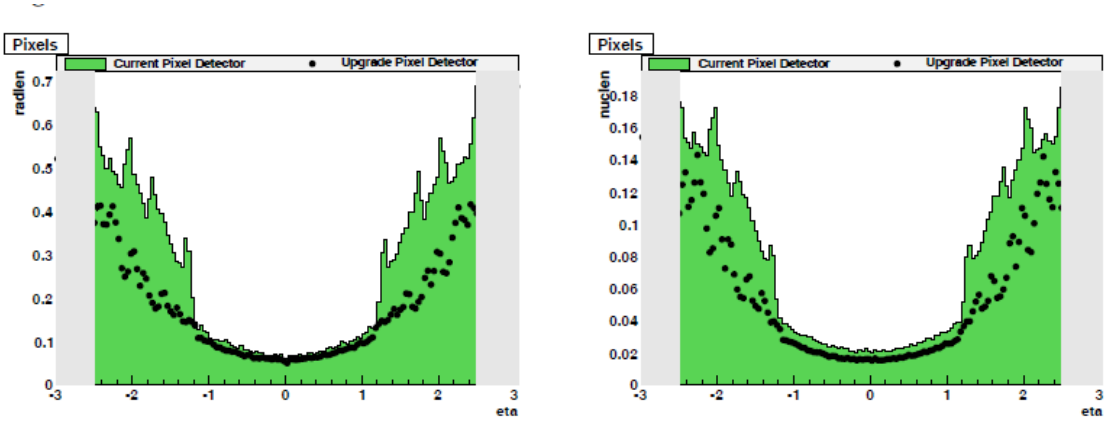

Fig.4 Material budget of the present detector in comparison with the upgraded detector both in units of radiation lengths and interaction lengths as function of pseudorapidity η.

Concerning the tracking efficiency, in addition to material budget, it is also important to consider data loss. In order to reduce the data loss a new front-end chip is under design; if the design goal of the chip will be achieved, the performances in terms of data loss will reach the level shown in Fig.5. As reported from the simulation, in the worst scenario (layer 1 luminosity 2 x 10^{34} cm^2 s^{-1} and 50 ns bunch spacing) the data loss will go from 50% in the present detector to 4.76 % in the new pixel detector.

Considering the change in the layer structure and the reduction of material and data loss, the overall tracking efficiency and fake rate have been simulated in two physical situations. In fig.5 and 6 are shown the results for a dimuon pair event and a dijet event produced by tt-bar with the upgraded detector in various luminosity scenarios. The simulations show that in the dimuon case the fake rate is low in both detector versions but the data loss is much lower at higher luminosity in the upgraded detector especially in the region of low absolute pseudorapidity η. A similar behavior for the data loss is observed in the tt-bar case while for the fake rate it is evident an

improvement for all the pseudorapidity values mostly due to the reduction in the material budget.

Detector	Radius (cm)	% Data loss for ($cm^{-2}s^{-1}$ @ ns) 1×10^{34} @ 25	2×10^{34} @ 25	2×10^{34} @ 50
Current detector				
BPIX1	4.4	4.0	16.0	50.0
BPIX2	7.3	1.5	5.8	18.2
BPIX3	10.2	0.7	3.0	9.3
FPIX1 and 2		0.7	3.0	9.3
Upgrade detector				
BPIX1	3.0	1.19	2.38	4.76
BPIX2	6.8	0.23	0.46	0.93
BPIX3	10.2	0.09	0.18	0.36
BPIX4	16.0	0.04	0.08	0.17
FPIX1–3		0.09	0.18	0.36

Fig.5 Data loss percentage for the present and upgraded detector in various luminosity scenarios for all the detector layers.

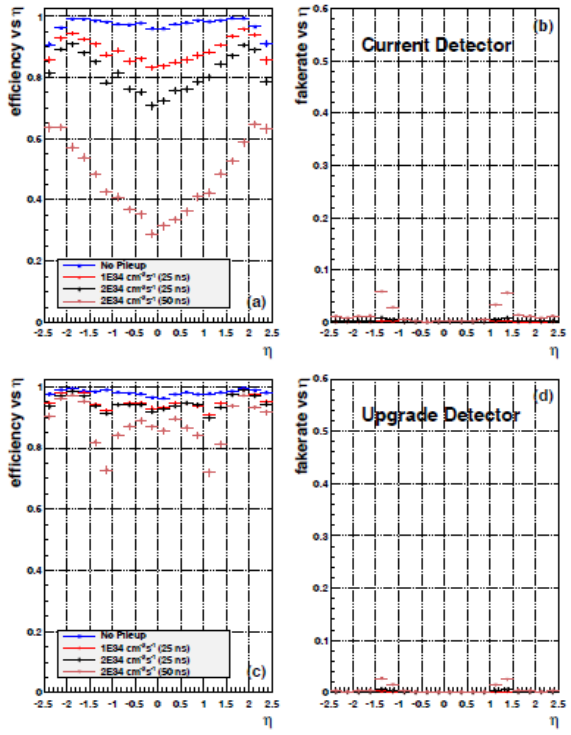

Fig.6 Tracking efficiency and fake rate for a dimuon event as a function of pseudorapidy for the present and for the upgraded pixel detector as a faction of η in various luminosity scenarios.

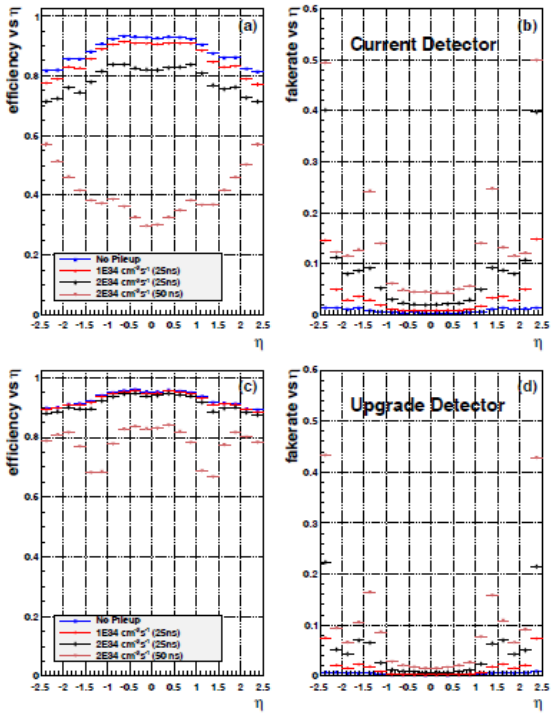

Fig.7 Tracking efficiency and fake rate for a tt-bar events as a function of pseudorapidy for the present and for the upgraded pixel detector as a faction of η in various luminosity scenarios.

3. Description of phase 1 pixel detector

The layout of the upgraded CMS pixel detector it is shown in Fig.3a. It composed of 4 layers of silicon sensor equipped with digital readout electronics in the barrel structure (BPIX) and 3 layers per side of endcap detectors (FPIX). This structure allows a 4-hit coverage for all tracks, in particular for values of $\eta < 1.3$ the tracks cross only the 4 layers of the BPIX structure and for $1.3 < \eta < 2.5$ the tracks pass through one or more layers of FPIX but still crossing 4 layers of pixel sensors.

The upgraded FPIX detector consists of two sections which are vertically separated with a left and a right set of half-disks on each side. The pixel modules are assembled on half-disk support structures which are mounted on a service half cylinder (HC). The pixel module radial coverage ranges from 4.5 to 16.1 cm. Cooling tubes and the readout electronics are placed on the half cylinders most of which will be located away from the sensors sensitive area.

The forward upgraded detector uses the module showed on Fig.8c, with 16 readout chips in a 2 x 8 ROC arrangement, the same as for the barrel. The modules are arranged radially on a light-weight substrate called "blade". There are a total of 56 modules (896 ROCs) per half-disk. Half-disks are divided into an outer ring with 34 modules and an inner ring with 22 modules.

Each blade on the outer ring is rotated by 20°, furthermore in order to obtain excellent resolution in both the azimuthal and radial directions throughout the FPIX acceptance angle for the inner ring, the blades are arranged in an inverted cone array

with the blades tilted by 12◦ with respect to the interaction point, combined with the 20◦ rotation. Figure 9 shows the structure of an half disk.

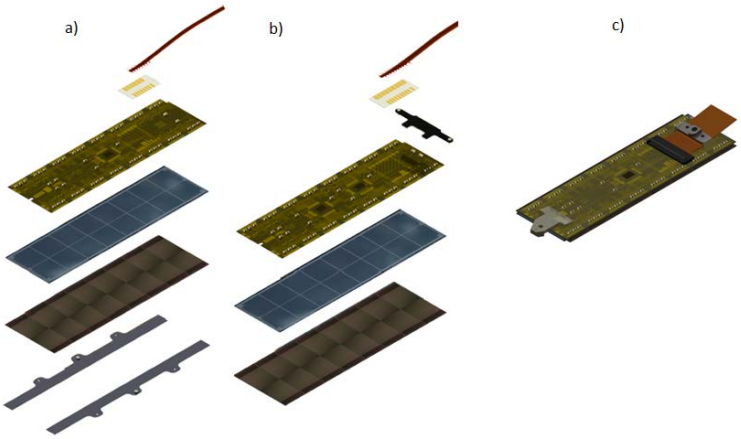

Fig.8 Layout of the pixel detector modules a) is for BPIX layers 2-4 it includes (from top to bottom) cable, connector, HDI, silicon sensors, ROCs and base strips b) module for BPX layer 1 it includes cable connector, carbon fiber holder, HDI (with 2 TBM), silicon sensor, ROCs, c) FPIX module assembled.

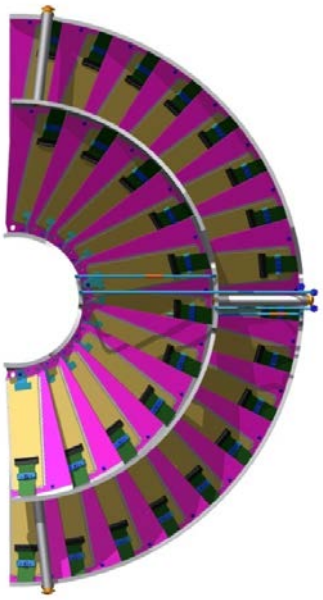

Fig.9 Half-disk of FPIX

The BPIX section configuration is shown in Fig. 3b. It assembled using two different modules configurations: one for layers 2 to 4 (Fig. 8a) and the other of layer 1 (Fig. 8b). The number of modules in the detector will range from 96 (12 facets) in the first layer to 512 (64 facets) in the fourth layer, for a total of 1184, each facet of the barrel is a row of 8 modules.

Each module is composed by a flexible cable and connector, an HDI (High Density Interconnect circuit) with one (or two in the case of the first layer) TBM (Token Bit Manager, a circuit that handles the readout sequence) onboard, a pixel sensor array

described in the previous section, the digital ROC array (Read-Out Circuit) and two base strips (replaced by a carbon fiber holder in layer 1) [4].

As already mentioned the two main improvement of the upgraded pixel detector are the reduction of the material budget and the reduction of data loss. This will allow the increase in the tracking efficiency and the reduction of fake rate.

The reduction of the material budget is mostly due to: a) Removal of electrical/mechanical parts from the interface region between BPIX and FPIX. b) The adoption of a new detector cooling technique based on biphasic CO_2 coolant that uses less material for tubing and a reduced amount of fluid compared with the previously used monophasic C_6F_{14}. c) A more optimized support mechanics.

Concerning the reduction of data loss it has been achieved by the adoption of a new fully digital ROC compared to the previous analog ROC; a comparison between the performance of the two chips is shown Fig.10.

	PSI46V2	PSI46DIG
ROC size	7.9 mm x 9.8 mm	7.9 mm x 10.2 mm
Pixel size	100 μm x 150 μm	100 μm x 150 μm
Smallest radius	4.3cm	2.9cm
Settable DACs / registers	26 / 2	19 / 2
Power Up condition	not defined	default values
pixel charge readout	analog	digitized, 8bit
Readout speed	40 MHz	160 Mbit/s
Time stamp Buffer size	12	24
Data Buffer size	32	80
Output Buffer FIFO	no	yes
Double column Speed	20 MHz	20 MHz (40 MHz)
Metal layers	5	6
Leakage current compensation	yes	no
in-time threshold	3500 e	$<$ 2000 e
PLL	no	yes
Data loss at max Operating flux	$\sim$3.8% at 120 MHz/cm^2	1.6% at 150 MHz/cm^2 ($\sim$3% at 580 MHz/cm^2)

Fig.10 Comparison between the performance of the analog ROC (PSI46V2) used in the current pixel detector and the new digital ROC (PSI46DIG) used in the upgraded detector

A notable feature of the new chip is the reduced data loss at high acquisition rate and the possibility of using a lower signal threshold in order to compensate the reduction in the signal amplitude due to the progressive deterioration of the silicon sensor caused by radiation damage.

4. Conclusions

The upgraded silicon pixel detector, currently under development by the CMS collaboration will work adequately in the high luminosity environment of the upgraded LHC peak luminosity of 2 x 10^{34} cm^{-2} s^{-1} at 25 ns bunch crossing (or at 50 ns bunch crossing) that will be available stating from year 2017 up to year 2023. The upgraded detector will also be able to compensate the loss of charge collection efficiency due to radiation damage that will occur during these years of operation. The schedule for this detector foresees the development and the production of the new ROC, TBM and HDI from now till mid 2014, from end 2014 to early 2016 the new modules will be manufactured and integrated on the mechanical structures, and finally after a period of testing the new detector will be inserted in late 2016 (or early 2017) within the CMS

apparatus for commissioning and operation. For this important construction challenge the CMS pixel-detector collaboration, subdivided into national consortia, has set-up an appropriate task sharing. In particular the Italian consortium that will build, test and commission one half of the third layer of the BPIX detector is organized as follows: INFN Pisa will test the silicon sensor arriving from the production and INFN Padova will test the ROCs. INFN Pisa will supervise and test the bump bonding between the sensors and the ROCs. INFN Catania will assemble and test the HDI adding the cables and the TBMs. INFN Bari will build the complete module taking the bare module (ROC assembled with sensor) from Pisa and the assembled HDI from Catania. INFN Perugia will qualify and test the final modules and will collaborate with Pisa to the final integration of the modules in the mechanical structure.

References

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