PROCEEDINGS OF SCIENCE

Operational Issues of the Present CMS Pixel Detector

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The core of the CMS experiment is a three-layer pixel detector. Installed in 2008, the CMS pixel system is essential for track seeding and reconstruction of secondary vertexes. The presentation will summarize the operational experience of the first four years of collisions at the LHC. We will present the measured performance evolution as the instantaneous luminosity delivered increased by several orders of magnitude, including dynamic data-losses, efficiency and resolution. The focus of the presentation will be on the operational challenges encountered to present. Moreover the impact of radiation on on-detector electronics, including both single-event upsets and cumulative changes in performance, are discussed. Leakage current and depletion voltage are monitored with increasing fluence. Methods for addressing the challenges of these measurements in the context of ongoing detector operations are discussed.

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1. Introduction

The pixel detector plays a key role in all aspects of the Compact Muon Solenoid (CMS) [1] physics program, providing high-precision position information needed for charged particle tracking [2] in the dense environment of Large Hadron Collider (LHC) collisions. It is used for the initial track seeding and is vital for high-precision reconstruction of secondary vertexing.

The pixel detector provides coverage in the pseudorapidity (η)[1] range $|\eta| < 2.5$. The detector consists of three cylindrical barrel (BPIX) layers centered at the nominal LHC interaction point, with two forward pixel (FPIX) disks at each end. The barrel layers extend 56 cm along the LHC beam, and are placed at radii of 4.3, 7.2, and 10.8 cm. The endcap disks have inner radius 6 cm and outer radius 15cm, and are placed at 34.5 and 46.5 cm along the LHC beam (z) axis on each end of the barrel. The thickness of the active silicon is 285 μm. A schematic of the pixel detector and its coverage in η is shown in Figure 1. Each pixel has a dimension of 100 μm $\times$ 150 μm; there are a total of 48 (18) million pixels in the BPIX (FPIX).

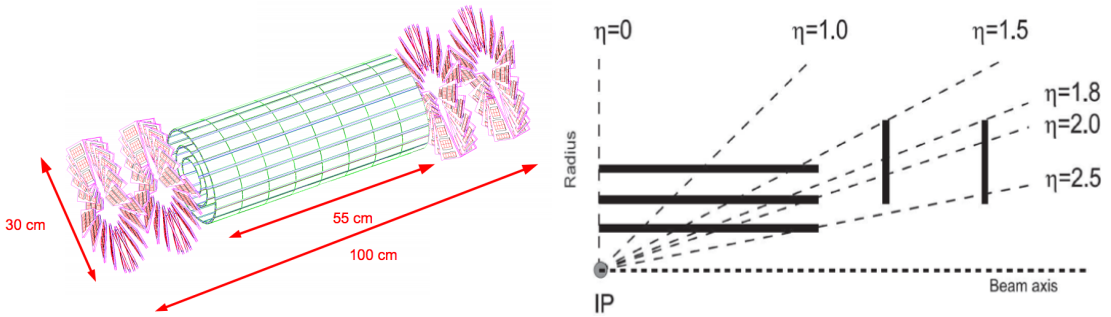

Figure 1: Left: a schematic of the pixel detector layout. Right: the coverage of each barrel layer and disk in pseudorapidity.

The detector uses an analog readout, in which individual readout chips (ROCs) are read sequentially when a trigger is received. Each of the detector's 15840 ROCs is connected to an array of 52 $\times$ 80 pixels. Zero-suppression is implemented at the level of individual read-out circuits in the ROC, with only those pixels that register hits being read out; each has an individual address and pulse height reading attached. Pulse heights are used for charge sharing, allowing a hit resolution much better than that intrinsic to the pixel sizes to be achieved, as described in Section 4. Signals are transmitted from the pixel detector to the counting room via a total of 1320 optical readout channels.

2. Detector status

The pixel detector has been highly reliable and successful in operation since its installation in 2008. In 2012, when the overall CMS data-taking efficiency was an excellent 94%, pixel operational issues accounted for only 9% of CMS downtime.

[1]CMS uses a right-handed coordinate system with the z-axis pointing along the LHC counter-clockwise beam direction, the x-axis pointing toward the center of the ring, and the y-axis pointing upward. The azimuthal angle θ is measured around the beam axis and the polar angle ϕ is measured from the z-axis. The pseudorapidity η is defined to be $-\ln(\tan\frac{\theta}{2})$.

Almost all detector channels are operational, with only 3.6% of ROCs unavailable for readout. One major type of lost channel is those producing an incorrect pulse shape, which results in their signal being unidentified within the analog pulse train. One entire optical channel in the FPIX is lost due to a broken laser driver. Finally, several barrel modules make use of an older ROC design with an occasional readout error that requires them to be reset [3]; as increasing luminosity during 2012 caused these errors to become more frequent, it was necessary to disable them.

It is anticipated that all unavailable channels will be repaired during the upcoming 2014-15 LHC shutdown. The capability to efficiently remove, repair, and reinstall components of the pixel detector was already been demonstrated in 2009, when channels with bad electrical connections accounting for 5.3% of the FPIX were recovered [4].

3. Calibration and scans

A set of calibrations is performed weekly in order to ensure the smooth functioning of the readout system. The baseline level of the optical receiver is adjusted in order to account for temperature-induced variations, with additional small adjustments made automatically. The address level calibration verifies that there is good separation between the ADC count ranges corresponding to each address level used by the optical readout. The efficiency of a subset of pixels as a function of injected charge is measured. The gain calibration confirms that there is a linear response of the ADC count with injected charge.

Further calibrations are run a few times a year to determine the full range of readout settings, including:

- the bias and gain of the optical readout levels;
- the levels of the black (baseline) and ultrablack (used for header) signals at each readout step;
- the delay for sending and returning commands;
- charge injection timing and response;
- ROC-level analog pulse height; and
- individual pixel pulse heights.

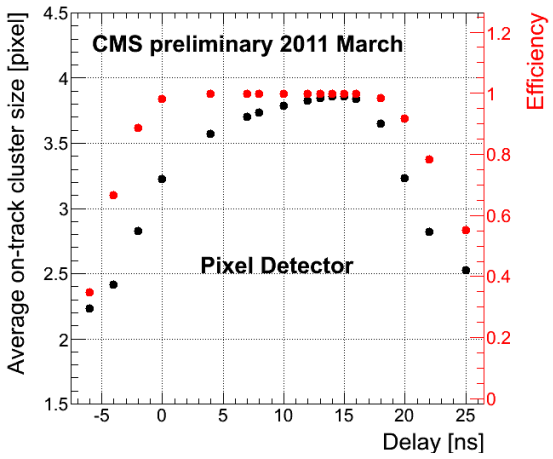

Figure 2: In the timing scan, pixel hit efficiency and cluster size are measured as a function of readout delay settings, as described in the text. The red points correspond to the efficiency, and the black to the cluster size.

Finally, the ROC analog voltage may also be adjusted, which changes the pulse rise time and hence the difference between the charge required for a pixel to reach threshold and the charge required for it to reach threshold within one bunch crossing. This calibration was performed at the start of 2012 to account for a change

in detector operating temperature (from about 17°C to about 10°C). It has also been necessary to adjust the analog settings every few months during 2012 due to the changes in analog current described in Section 5.3.

Two additional scans are conducted regularly to ensure good performance of the detector. One is the timing scan, in which readout delay settings are varied during LHC running to confirm that they are on plateau for good efficiency, as illustrated in Figure 2. The high voltage bias scan, in which hit efficiency is measured as a function of the bias voltage during LHC running, is discussed in Section 5.2.

4. Performance

Pixel hit efficiencies are determined by measuring missing hits on reconstructed tracks during LHC running. The efficiency for working ROCs is above 99.5% for all layers, as shown in Figure 3. Small inefficiencies have been observed, due to increased detector occupancy, as the LHC luminosity increases.

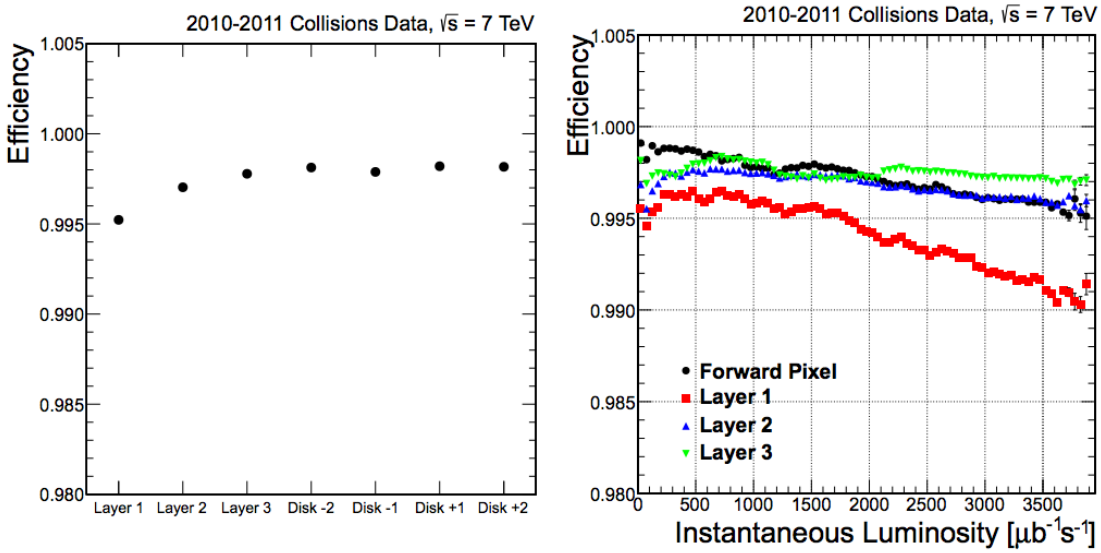

Figure 3: The efficiency of pixel hit-finding in 2010-2011 data, separated into individual barrel layers and disks (left) and shown as a function of instantaneous luminosity (right).

Pixel hit resolutions are measured using the triplet method, in which tracks with 3 hits in the barrel are extrapolated to Layer 2 using the Layer 1 and 3 positions and angles. The residual in both the precision ϕ direction and in the z direction may then be measured and the resolution computed, as shown in Figure 4. Hit resolutions may also be determined for tracks that contain multiple hits on the same layer due to overlapping regions; these yield consistent results.

5. Impact of radiation damage

From its inception, the design of the pixel detector focused on the ability to continue operation even after significant radiation damage due to LHC particle fluence. The sensors are produced

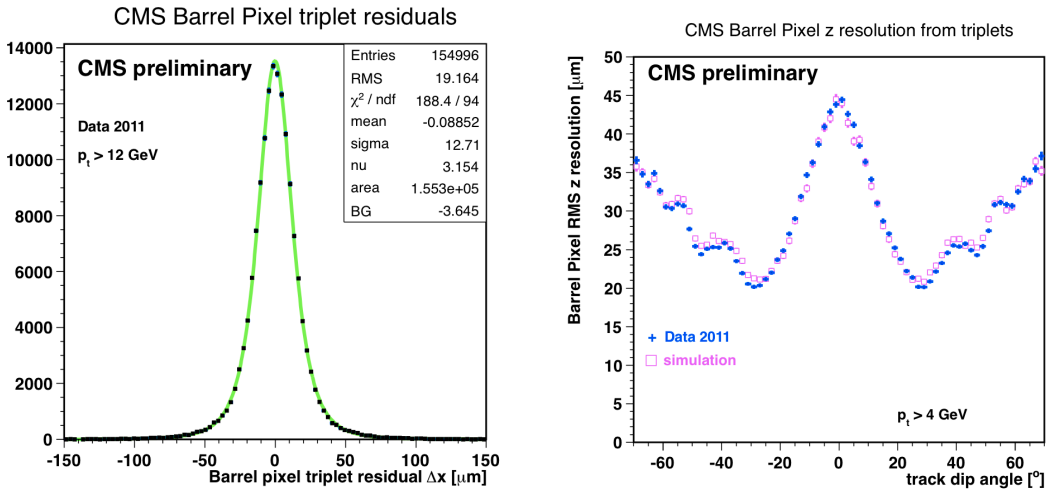

Figure 4: Left: barrel hit residuals in the precision ϕ direction, measured using the triplet method as described in the text. Right: barrel hit resolutions measured in the z direction using the same method, as a function of track angle with respect to the silicon.

from silicon with high oxygen content in order to ameliorate the impact of damage to the silicon structure [5], and feature double-sided processing that allows hits to be read out even when the sensor can no longer be fully depleted.

Radiation damage is presently monitored through studies of the leakage current and depletion voltage evolution. Changes to the analog current in each ROC, correlated with integrated luminosity, have also been observed. Furthermore an increasing number of disruptions in on-detector pixel electronics have occurred with increasing luminosity; these may be attributed to Single Event Upsets, i.e. bit flips in memory caused by ionizing charged particles.

5.1 Leakage current

Leakage current is measured in the pixel barrel, using readings from the high voltage power supplies, and compared to models of leakage current evolution in radiation damage. In order to facilitate comparison between experiments, measured leakage currents are normalized by the area of instrumented silicon and extrapolated to 0°C using the equation

$$I(T_{ref}) = I(T)\left(\frac{T_{ref}}{T}\right)^2 \exp\left(-\frac{E_g}{2k_B}\left[\frac{1}{T_{ref}} - \frac{1}{T}\right]\right)$$

where $E_g = 1.21$ eV. The leakage current varies as a function of azimuthal angle, due to an offset between the LHC beamspot and the center of the pixel detector. Due to this offset, the various detector channels have many separate radii, allowing a clear fit of the leakage current as a function of radius, as shown in Figure 5.

The leakage current averaged over each barrel layer is shown in Figure 6, as a function of integrated luminosity and of time in 2011-12. The data are compared to a parameterization adding exponential and logarithmic terms [6], which accounts for accumulated damage and for annealing, whose input is the fluence as predicted by a model of the CMS detector implemented in the FLUKA

program [7, 8]. This model produces good agreement with the data, after being scaled up by 40% for Layer 1, 50% for Layer 2, and 70% for Layer 3. The reasons for these discrepancies in scale remain under investigation, with possibilities including uncertainties in the operational temperature and incorrect particle content input to FLUKA.

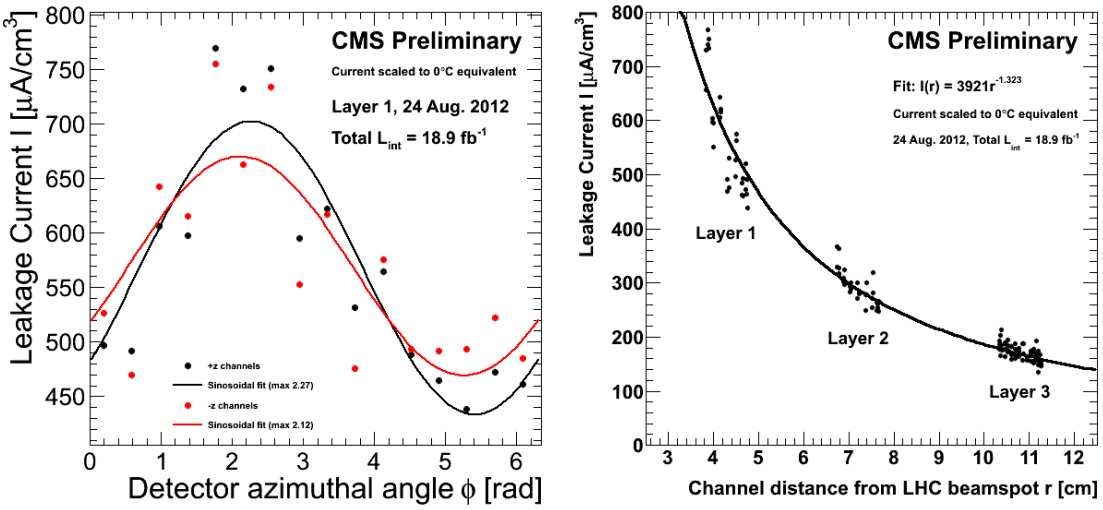

Figure 5: Leakage current as a function of azimuthal angle for Layer 1 (left), and as a function of distance from the LHC beamspot (right). For the azimuthal angle, red (black) points represent detector channels at positive (negative) z. The sinusoidal fit does not describe all differences between channels; for example, the alternation of channels closer and further to the beam spot within the layer can also be seen.

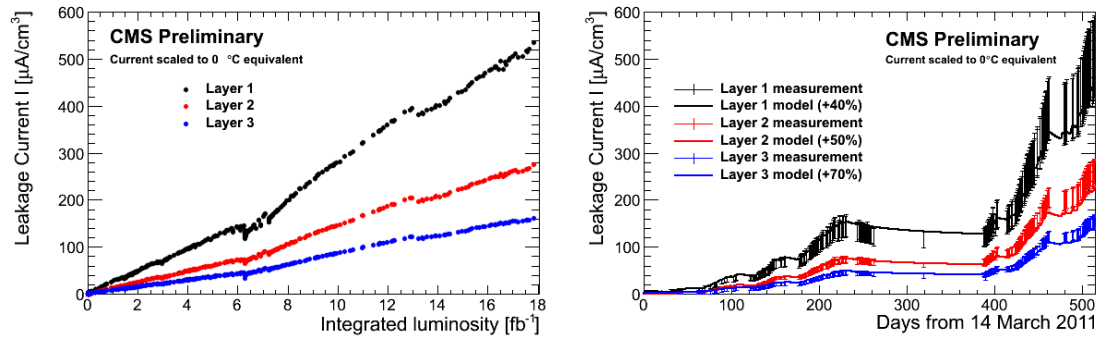

Figure 6: Average leakage current in each barrel layer as a function of accumulated integrated luminosity (left) and time in 2011-12 (right). The data at right are compared to a leakage current model as described in the text.

5.2 Depletion voltage

The depletion voltage is investigated by varying the bias voltage at which the detector is run during LHC operation, thereby changing the charge collection and hit efficiency. The hit efficiency measured in such scans, for particular channels in Layer 1 and 3, are shown in Figure 7. The 99% efficiency point can be qualitatively compared to the depletion voltage *prior to type inversion*.

Afterward, the pixel system's double-sided readout ensures high efficiency even if the detector is not fully depleted; thus, future measurements will use the voltage at which the most probable value of the collected charge becomes stable as a point for comparison. The evolution of one particular HV channel in Layer 1, as well as for modules at various z positions, is shown as a function of time in Figure 8. The data are compared to a parameterization using the Hamburg model for oxygenated silicon [9], with good agreement obtained. It can be seen that type inversion occurred in Layer 1 during 2012 running.

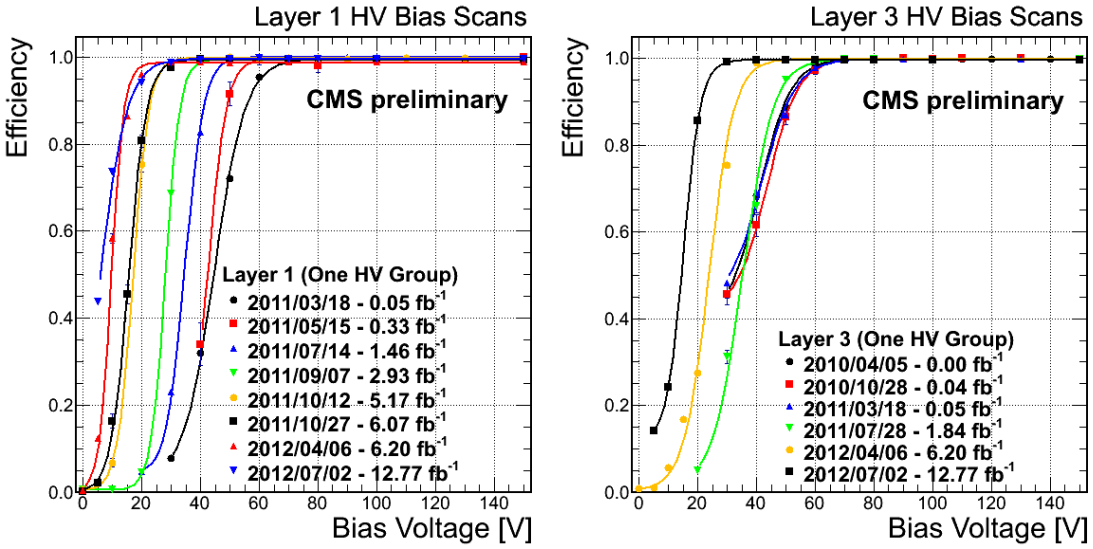

Figure 7: Hit efficiency results from the bias scan, taken at various luminosities, for Layer 1 (left) and Layer 3 (right).

5.3 Analog current

During 2012 running, it has been observed that the analog current drawn increases with time, necessitating analog recalibration every few months in order to avoid exceeding power supply limits. This effect was not anticipated. A possible mechanism by which it may have arisen is that the meaning of any given fixed analog voltage DAC setting has been changed; this may have been caused by bulk damage in a diode used as a reference voltage within the ROC. Work in modeling and understanding this effect is ongoing.

5.4 Single Event Upsets

In principle, bit flips caused by Single Event Upsets (SEUs) may occur in electronics at the pixel, ROC, or in higher-level on-detector electronics that organize many ROCs. In the last case, a significant fraction of the detector may be rendered non-operational until it is reset. Therefore, techniques for detection and recovery have been implemented in the pixel software. If a readout channel does not return data, or if too many synchronization errors are observed in too short a time, the CMS central trigger is stopped and all on-detector electronics at the ROC level and above is reprogrammed. If individual ROCs stop functioning during a run, they are recovered at this time, but immediate action is never taken based on individual ROC malfunction. Individual pixel

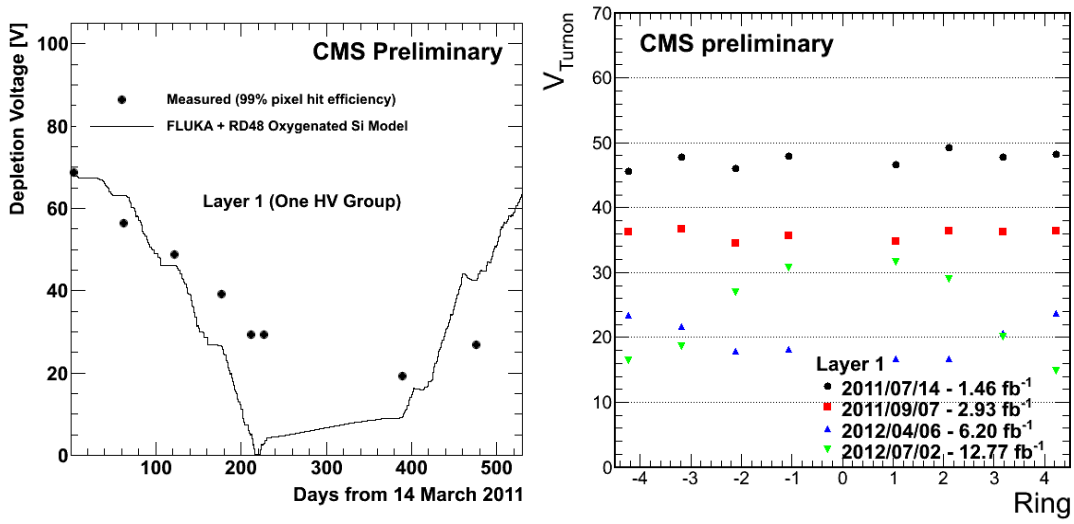

Figure 8: The voltage at which 99% hit efficiency is obtained, shown for one high voltage channel at left, and for modules at various z positions at right. (The ring number used for the axis label corresponds to the count of modules along the z axis, there being four modules along the length of both the positive and negative halves of the barrel. Thus ring -1 is those modules closest to the center in the $-z$ half, ring 4 is those furthest from the center in the $+z$ half, and so on.) The plot at left is compared to a model as described in the text.

errors due to SEUs represent too small a fraction of the detector to take action, so pixels are not reprogrammed. It should be noted that it is not presently possible to prove that errors recovered by this procedure are due to true SEUs, e.g. by reading back the configuration and identifying the impacted bit.

6. Conclusions

Pixel detector operation from installation in 2008 through 2012 has been very successful. The pixel detector accounted for only 9% of overall CMS downtime in 2012. Hit efficiency and resolution are excellent as expected. The progress of bulk silicon radiation damage, as measured by leakage current and depletion voltage, agrees broadly with expectations; there is ongoing work to understand and mitigate other aspects of radiation damage.

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