PROCEEDINGS OF SCIENCE

ATLAS FE-I4 ASIC

Lea Caminada[*], **Julien Fleury**[†], **Dario Gnani, Maurice Garcia-Sciveres, Frank Jensen, Yunpeng Lu**[‡], **Abderrezak Mekkaoui, Peyton Murray**
Lawrence Berkeley National Laboratory, 1 Cyclotron Road, Berkeley, CA 94720, USA
E-mail: lcaminada@lbl.gov

David Arutinov, Malte Backhaus, Marlon Barbero[§], **Xiaochao Fang**[¶], **Laura Gonella, Tomasz Hemperek, Michael Karagounis, Hans Krüger, Andre Kruth, David-Leon Pohl, Norbert Wermes**
Physikalisches Institut, Universität Bonn, Nussallee 12, D-53115 Bonn, Germany

Patrick Breugnon, Denis Fougeron, Fabrice Gensolen, Mohsine Menouni, Alexandre Rozanov
CPPM Aix-Marseille Université, CNRS IN2P3, Marseille, France

Roberto Beccherle, Giovanni Darbo

INFN Genova, Via Dodecaseno 33, IT-16146 Genova, Italy

Vladimir Gromov, Ruud Kluit, Jan David Schipper, Vladimir Zivkovic

NiKHEF, Science Park 105, 1098 XG Amsterdam, The Netherlands

Jörn Grosse-Knetter, Jens Weingarten
II. Physikalisches Institut, Universität Göttingen, Friedrich-Hund-Platz 1, D-37077 Göttingen, Germany

Martin Kocian

SLAC, 2575 Sand Hill Road, Menlo Park, CA 94025 MS 96, USA

The ATLAS FE-I4 ASIC is a novel pixel detector readout chip designed in a CMOS 130 nm feature size process. The chip is able to cope with high hit rate and withstand the harsh radiation environment in close proximity to the interaction point at LHC. FE-I4 will find its first application with ATLAS IBL, an additional innermost pixel layer scheduled for installation in 2013, but is also suited for the intermediate radii pixel layers for future upgrades. In this paper, the modular design concept of FE-I4 is introduced and its readout architecture, analog performance and radiation hardness are discussed. After the successful development of the first full-scale prototype version of the chip in 2010, the production version for IBL (FE-I4B) has recently become available. Here, we review the main design choices for FE-I4B and present first testing results.

The 21st International Workshop on Vertex Detectors
16-21 September 2012
Jeju, Korea

PoS(Vertex 2012)023

1. Introduction

In the ATLAS experiment at the CERN LHC a 3-layer silicon pixel detector allows for high precision tracking in close proximity to the interaction point. It operates in a challenging environment characterized by high track multiplicity and heavy irradiation. This requires fast detectors with high granularity and able to withstand high radiation levels. The LHC started operation in 2010 at a center-of-mass energy of $\sqrt{s} = 7\,\text{TeV}$, before the energy was raised to $\sqrt{s} = 8\,\text{TeV}$ in 2012. It currently runs with a bunch crossing separation of 50 ns and reached peak luminosities of up to $7.7 \cdot 10^{33}\,\text{cm}^{-2}\text{s}^{-1}$. The ATLAS pixel detector has shown an excellent performance so far and played a key role in the reconstruction of high quality physics data [1].

To maintain this performance at the higher luminosities expected in the coming years (up to $2 \cdot 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$ by the year 2020), a forth pixel layer will be added as innermost layer to the current pixel system. The so-called insertable B-layer (IBL) is scheduled for installation during the first long LHC shutdown in 2013 [2]. The IBL will be placed at a radius of 3.2 cm and inserted together with a new beampipe to fit into the small volume limited by the inner radius of the current B-layer at 5 cm. The readout chip used in the current pixel detector (FE-I3) has not been designed to operate at the hit rates present at such a small radius. At the expected IBL occupancy at a luminosity of $2 \cdot 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$ the efficiency of FE-I3 decreases dramatically which is mainly caused by the saturation of the column drain readout architecture [3]. The FE-I4 ASIC has been designed to overcome these limitations. It incorporates a novel readout architecture based on local hit processing and data storage which allows for high rate operation with very low inefficiency. At the same time the improvements in the hit processing lead to a significant reduction in the digital power consumption of the chip. The FE-I4 uses the CMOS 130 nm feature size process which offers a higher radiation tolerance thanks to the use of thinner gate oxide transistors. The FE-I4 chip is specified for a radiation tolerance of up to 250 Mrad. Furthermore, the 130 nm technology shows good analog performance and is easily accessible through vendors.

With these characteristics the FE-I4 design is also suited to be used in the outer layers of future pixel detector upgrades for HL(High Luminosity)-LHC. Design concepts of these detectors are currently under discussion within the ATLAS collaboration and R&D projects are ongoing.

This article is organized as follows: In section 2 the FE-I4 design concept and readout architecture are introduced. The main developments from the first full-scale prototype version of the chip (FE-I4A) to the production version for IBL (FE-I4B) are reviewed. The powering options for IBL operation together with the first testing results of the powering scheme are presented in section 3. Section 4 discusses the performance of the pixel array and summarizes the main results of the characterization of the analog pixel obtained by single chip testing, while section 5 focusses on the wafer level testing procedure and results. Conclusions are drawn in section 6.

*Speaker.
†Visitor from LAL - Laboratoire de l'Accélérateur Linéaire, Orsay, France
‡Visitor from IHEP - Institute of High Energy Physics, Beijing, China
§now with CPPM Aix-Marseille Université, France
¶now with IPHC Strasbourg, France

2. FE-I4 design

FE-I4 accommodates a large array of 26880 pixels arranged in 80 columns by 336 rows. The pixel size of $50\times250\,\mu m^2$ is smaller compared to FE-I3 which improves the resolution in the coordinate along the beam direction and at the same time lowers the pixel occupancy. Even though the FE-I4 periphery provides significantly more digital functionality with respect to FE-I3, the active area of the chip has been increased to almost 90%. Thanks to the complex digital functionality the chip can be operated in the detector without the need of an additional module controller chip. Considering also the large size of the chip, this allows for a simpler module design which reduces the material used in the detector as well as the cost of module production. Some key features of the FE-I4 design are compared to its predecessor FE-I3 in Table 1.

Table 1: Key features of the FE-I4 design compared to its predecessor FE-I3.

	FE-I3	FE-I4
Year	2003	2010
Feature size	250 nm	130 nm
Chip size	$7.6\times10.8\,mm^2$	$20.2\times18.8\,mm^2$
Active area	74%	89%
Size of pixel array	18×160 (2880)	80×336 (26880)
Pixel size	$50\times400\,\mu m^2$	$50\times250\,\mu m^2$
Number of transistors	3.5 M	87 M

The analog pixel of FE-I4 [4] is based on a two stage architecture featuring a pre-amplifier with leakage current compensation circuitry AC-coupled to a second amplification stage. The amplification stage is followed by a comparator with global and local threshold adjustment. Each pixel has 13 configuration bits for masking, threshold setting, adjustment of the feedback current and local test charge injection. If a signal above threshold is detected, the time-over-threshold (ToT) is measured which is proportional to the charge thanks to the linear return to baseline.

The analog pixels are arranged in double columns and the readout of 4 analog pixels is organized in a common digital region (see Figure 1). The hit processing and the ToT measurement happen independently for each pixel locally within the digital region. There are five ToT memories per pixel to store the hit information during the trigger latency. Due to space constraints and to reduce pileup from out of time hits, the ToT resolution has been reduced to 4 bits. Five latency counters per region are shared by the 4 pixels. Each latency counter is mapped one-to-one with four ToT memories. If a pixel records a hit above threshold a latency counter is started and the ToT of all pixels in the region is recorded.

The advantage of this regional architecture is the reduction of the data transfer to the periphery. Since the trigger verification is performed within the region, hits that do not belong to a trigger are discarded before being sent to the periphery. This results in only 0.25% of all hits being transferred. Therefore the dead time during the column readout is significantly decreased and at the same time a lower power consumption is achieved.

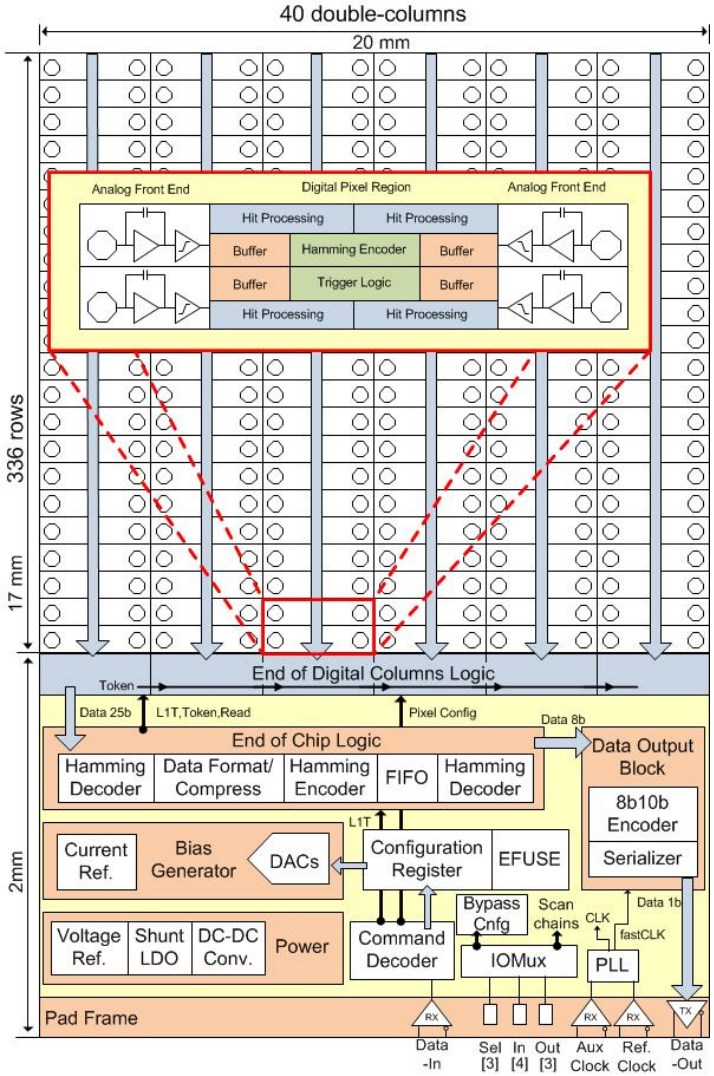


Figure 1: Schematic view of the FE-I4 readout architecture. The pixels are arranged in double columns and 4 analog pixels share a common digital region.

In contrast to the column drain architecture implemented in FE-I3, the local readout concept of FE-I4 simply scales to larger size pixel arrays and thus serves as a baseline for future chip design using advanced technologies, like CMOS 65 nm feature size or 3D integrated Tezzaron-Chartered 130-nm technology [5].

As an additional benefit the arrangement of pixels in 4-pixel digital regions provides a handle on time walk effects. Simulations show that hits with small amplitudes in most cases happen in close proximity to hits with large amplitudes. Hence, in FE-I4 small hits are associated to big hits based on position rather than on timing information. The latency counter of the digital region is triggered by big hits and uses a two clock cycle window to associate small hits in neighboring pixels to big hits. The discrimination between small and big hits is adjustable in the configuration. Thereby FE-I4 offers a digital time walk correction which allows to lower the analog current in the pixel preamplifier.

The readout of the hit information stored in the pixel digital regions is organized by a token mechanism running through the double columns. The output data consists of the pixel address together with the ToT information of the hit pixel and its neighboring pixels. The readout of the double columns happens sequentially as there is only one readout token distributed from the end of double column logic (EODCL). The data from the EODCL is then received by the end of chip logic (EOCHL). The EOCHL adds the trigger and bunch crossing information, reformats the data stream and passes it to the data output block (DOB). The DOB performs 8b10b encoding [7] as well as 160 Mb/s serialization before sending the output data to the data acquisition system. The 160 MHz clock needed in the DOB is generated by a PLL clock multiplier block that is also integrated in the chip periphery.

Many functions of the logic blocks in the periphery are programmable and the configuration is stored in global registers organized as a RAM block of 16-bit words. The global configuration registers as well as the pixel configuration registers are programed via the Command Decoder block (CMD). Figure 1 shows a schematic view of the FE-I4 chip periphery. A more detailed description is given in [8].

The first full scale prototype chip design called FE-I4A was submitted for production in summer 2010. 40 wafers of 60 chips were produced and the performance of the chip was evaluated in detailed studies. Very promising results were obtained and the functionality of all basic building blocks could be confirmed [9]. Furthermore, FE-I4A based modules with planar as well as 3D silicon sensors were built. They were characterized in laboratory tests before and after irradiation and were successfully operated in testbeams and during cosmic data taking. The results of the module testing are discussed in [6].

Thanks to these results the design of FE-I4B, the production version of the chip for IBL, was possible on a very short time scale. Since the design of the analog pixels and the new regional readout architecture have been validated successfully in FE-I4A, modifications for FE-I4B mostly concern the chip periphery. The modular structure of the FE-I4 periphery facilitates changes in the design and most of the building blocks (e.g. EODCL, CMD, DOB, PLL) could be adopted without any changes for FE-I4B.

Major changes were made to the design of the EOCHL. Some additions were needed in order to fulfill the requirements of the IBL data acquisition system, other design changes were implemented to fix circuits with faulty logic. Amongst others, the size of the bunch crossing and trigger counters was increased (to 13 and 12 bits, respectively), logic was added to allow for a programmable event truncation, the implementation of the counter of skipped triggers was corrected and the read-back functionality of the pixel configuration was enabled. Furthermore, the range of some DAC values needed adjustment and the centering of the current reference (nominal at 2 μA) was improved.

The redesign of FE-I4B also allowed to include new building blocks for monitoring and calibration purposes (e.g. GADC, temperature sensor, circuit for the measurement of the injection capacitance). The final design choices for the chip powering during IBL operations are discussed in the next section.

The functionality of these new and complex features (together with the existing ones) has been validated by detailed simulations. After deriving a netlist directly from the top level schematics, a system verilog model of the full chip was run within a digital test bench. This provides a framework

to study the behavior of the chip operating in different modes. Tests include chip configuration, data flow, event and trigger management as well as exception handling. Furthermore, physics events were generated and the response of the chip was simulated in runs which lasted up to a few seconds. The digital test bench has proven to be very effective in tracing down errors in the design and represents an invaluable tool for verification.

The submission of the FE-I4B design took place in September 2011 and first wafers have become available only a few months later. The preliminary results of the first diced chip and wafer level test with FE-I4B are discussed in the following.

3. Powering scheme

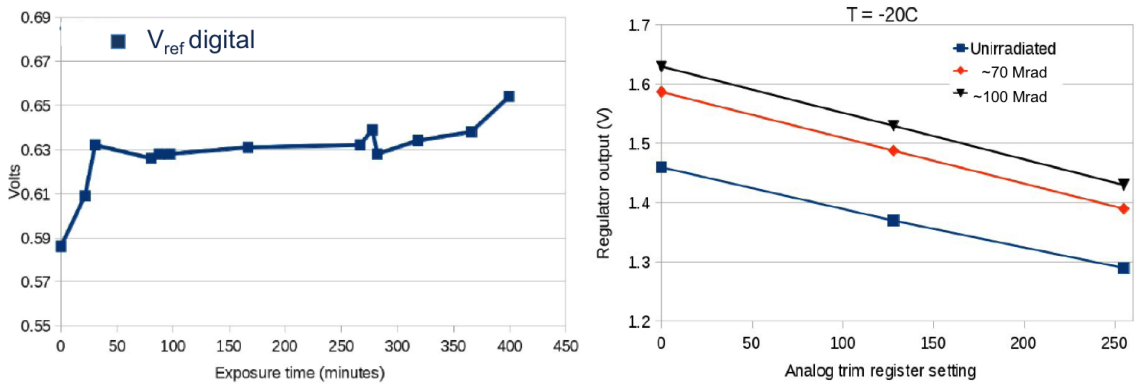
The nominal operating voltages for FE-I4 are 1.2 V for the digital supply and 1.2-1.5 V for the analog supply. The power consumption in the digital region has been measured as a function of memory occupancy and an excellent agreement with the value predicted by simulation has been obtained. At the expected IBL occupancy the digital region has a power consumption of about 24 μW. The total digital current in the chip is about 110 mA. The analog current is dependent on user optimization of the bias settings. As currently optimized for IBL operation the analog current amounts to about 350 mA. This results in a total power consumption of approximately 180 $\mathrm{mW/cm^2}$.

FE-I4B can be operated in two modes, either by directly connecting to the internal powering nets, or by the use of voltage regulators[1]. The former option has been maintained in order to allow for testing flexibility, while the latter is intended for IBL operation. FE-I4B includes two in-chip low drop out (LDO) regulators for analog and digital voltage supply operated in partial shunt mode [10]. This mode of operation is used to minimize transients in voltage based powering schemes where the load current is not constant.

FE-I4B provides two options for each digital and analog reference which will be denoted *voltage reference* and *current reference* in the following. The voltage reference is a band gap voltage circuit powered from the analog regulator input that produces a constant output voltage. The voltage reference circuit is a new addition to FE-I4B and has been thoroughly tested as soon as the first chips became available. The reference voltage has been measured during proton irradiation and an undesirable voltage increase has been observed as shown in Figure 2(a). Assuming the linear trend continues for higher dose values, this could present a possible danger for the front end if this reference voltage option were used stand-alone in IBL.

The current reference is derived from the 2 μA master current reference and suitable internal resistors. It results in a maximum output voltage of 1.65 V that can be regulated to lower values using trim down configuration registers. Since the master current reference is powered from the analog regulator additional startup circuitry is needed to ensure proper functionality as soon as power is applied. However, problems at startup have been observed during power cycling tests at low temperatures caused by the trim bits being in an undefined stage if the voltage turn on is too slow.

[1] FE-I4A also includes a divide-by-two DC-DC voltage converter. Despite promising testing results, this technology is not yet mature for the use in a project on the time scale of IBL. The DC-DC converter has been removed from FE-I4B to make room for new circuits and wire bond pads.



(a) (b)

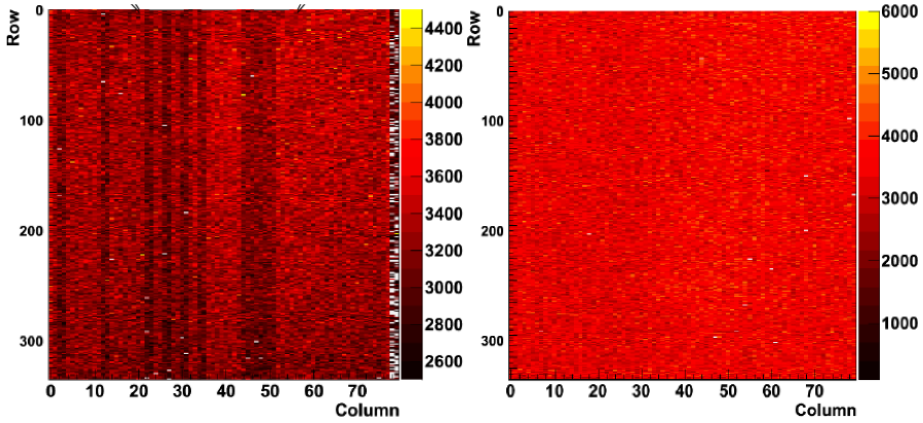
Figure 2: (a) Measured increase of band gap reference voltage as a function of exposure time during 800 MeV proton irradiation. (b) Analog regulator output voltage as a function of the setting of the trim down configuration register. Here the output of the current and the voltage reference are tied together. The analog regulator voltage is measured before and after proton irradiation.

An optimal solution for the analog voltage reference was found by tying together the outputs of the voltage and the current reference. This leads to an additional current being present at startup and thereby resolves the powering issues at low temperatures. Tests confirm a reliable operation at temperatures as low as -60^0C. Moreover, the tuning capability is preserved and the tuning range guarantees safe operation after irradiation as shown in Figure 2(b). The proper functionality at startup of the analog regulators permits the use of the current reference option for the digital voltage regulator. This powering scheme has been be adopted for IBL operation.

4. Performance of the pixel array

In FE-I4A, columns having pixels with different feedback capacitor or discriminator design were included to compare their performance. For 16 columns the baseline metal-metal feedback capacitor has been replaced by a Vertical Natural Capacitor (VNCAP). The value of this capacitor determines the gain and therefore affects the threshold of the channel. This is clearly visible in the FE-I4A threshold distribution before tuning shown in Figure 3(a). A low standby current discriminator is used in two FE-I4A columns to study a possible power reduction. In both cases the baseline design performs equally well as the proposed alternatives. Hence, the baseline design was adopted for FE-I4B to make the pixel array uniform (see Figure 3(b)).

The analog pixel shows an excellent performance: Despite the large pixel matrix, precise tuning is possible with a dispersion of less than 30 e^- at a threshold of 3000 e^-. Low threshold operation was demonstrated for FE-I4 modules with both planar silicon and 3D sensors and threshold of around 1400 e^- were achieved with a noise occupancy of the order of 10^{-8}. The noise measured in bare chips without sensor load is about 100 e^- and increases to about 150 e^- in assemblies with sensors.



(a) FE-I4A (b) FE-I4B

Figure 3: Untuned threshold distribution in (a) FE-I4A and (b) FE-I4B. The preferred column design of FE-I4A is adopted for FE-I4B to make the pixel array uniform.

FE-I4 includes a pulse generation circuit and injection capacitances to emulate charge deposition in the pixels. In FE-I4A the charge calibration was obtained indirectly based on the charge deposition in the sensor in source measurements. This resulted in a large uncertainty of the order of 20% due to systematic effects and the limited knowledge about the charge collection efficiency of the sensor. In FE-I4B dedicated circuitry for the measurement of the injection capacitances has been added to allow for an absolute charge calibration with a significantly smaller uncertainty. The measurement of the injection capacitances of 530 chips results in a mean value of 6.0 ± 0.2 fF to be compared to 5.7 fF predicted by simulation. In order to use this information in an optimal way, the value of the injection capacitances will be determined during wafer probing for each chip used for IBL production.

The radiation tolerance of FE-I4 has been verified in bare chip irradiations (both FE-I4A and FE-I4B) with 800 MeV protons at Los Alamos to doses up to 200 Mrad averaged over the whole chip. All chips could still be operated after irradiation. The analog performance proved satisfactory. The threshold dispersion in the pixel array is hardly affected by irradiation and the noise increase is moderate at a level of 15–20%. No systematic effects were observed.

The SEU hardness of the pixel configuration registers was studied during a dedicated irradiation campaign at the CERN PS with 24 GeV protons. Also for the pixel latch design two different versions are integrated in FE-I4A for testing purposes: 32 double columns use a DICE latch structure with linear NMOS and PMOS, the remaining 8 double columns use a more complex design with an enclosed NMOS, linear PMOS and guard ring structure that has been derived from earlier studies to increase SEU resistance by separating sensitive pair nodes [11]. From the measurements of FE-I4A at the CERN PS a cross section for SEU events of $1.1 \cdot 10^{-15}\,\mathrm{cm}^2$ was derived for the improved latch design which presents a reduction by a factor of 30 compared to the default design [12]. Consequently, the choice was made to use the more complex design for FE-I4B.

5. Wafer probing

38 FE-I4B wafers are needed for IBL construction including contingency. All of these wafers haven been received and testing is ongoing. The preliminary results of the wafer probing based on 30 wafers are presented in this section.

The wafer probing for IBL production is performed in-house while more basic tests of the digital functionality (IDDQ, scan chains, shmoo plots) are carried out by an external company. The testing procedure at wafer level includes chip calibrations, testing of the powering scheme, functionality of the chip digital periphery and pixel array as well as characterization of the analog performance.

During the chip calibration the proper setting of the trim bits for the master current reference is determined to achieve a current close to the nominal value of $2\,\mu$A. To allow for safe operation at startup of the power, the current reference trim bits have been implemented as wire bond pads. The centering of the current reference around $2\,\mu$A was found to be non ideal in FE-I4A and has been improved in FE-I4B. For FE-I4B a value of $2\,\mu$A with a spread of $0.2\,\mu$A has been determined during wafer probing.

The current consumption of the chips is measured in different configurations (minimal and default current setting) and during full digital activity. About 9% of the chips have too high currents and cannot be operated at all. For another 11% of the chips the currents measured after configuration or during operation show a large deviation from the core of the distribution and therefore do not comply with the quality criteria for IBL production.

The functionality of the global configuration registers is established by sending repeated read/write commands. The registers are very reliable and the failure rate is less than 1%. Similarly the read/write capability of the pixel registers is ensured.

In a next step, the performance of the pulse generator and the injection delay circuit is evaluated. About 4% of the chips fail these tests, either because the range of injected pulse sizes is not optimal, or because the delay circuit response is not monotonic. For the chips passing this testing stage, the injection pulse calibration as well as the measurement of the injection capacitances is performed.

The digital readout logic is tested in great detail to verify the data processing in the readout chain. On the level of the 4 pixel digital regions, all latency counters and hit buffers are tested. The analog performance is assessed based on the result of threshold and noise measurements for each pixel. The measured threshold and noise distribution are in good agreement with the expectations. Tight quality criteria have been assigned for IBL production and a chip is only accepted if less than 0.2% of the pixels show errors during any of the tests. This is the main reason for yield loss and affects 23% of the chips.

As a preliminary result an average yield of 61% has been obtained. Considering the large size of the chip this is a very good result and creates confidence in the reliability of the production process.

6. Conclusion

With the FE-I4 design a new generation of pixel detector readout chips is available. It incor-

porates an innovative readout architecture and sets new standards concerning readout speed and radiation hardness. FE-I4 shows an excellent analog performance and is able to operate at thresholds well below 2000 e^- with low noise occupancy. Furthermore, FE-I4 keeps the promise of operating at lower power and reduces the cost of module production thanks to its large physical size and the reasonable wafer yield. It meets the design requirements for IBL and the production of FE-I4 based modules is well underway. This constitutes a key ingredient for the successful completion of the IBL project. The evolution of readout chip technology towards smaller feature size, higher rate and lower power initiated by the FE-I4 project is continued in view of the experimental conditions at HL-LHC and the FE-I4 design serves as a baseline for future developments using advanced technologies.

References

[1] M. Keil, *Operational Experience with the ATLAS Pixel Detector at the LHC*, these proceedings.

[2] M. Kocian, *ATLAS Pixel, Phase 0 (IBL)*, these proceedings.

[3] D. Arutinov et al., *Digital Architecture and Interface of the new ATLAS Pixel Front-End IC for Upgraded Luminosity*, IEEE Trans. Nucl. Sci. 56 (2009) 2.

[4] M. Garcia-Sciveres, *The FE-I4 pixel readout integrated circuit*, Nucl. Instrum. Meth. A 636 (2011) 155-159.

[5] A. Mekkaoui, *Front end circuits in newer deep submicron technologies: opportunities and challenges*, proceedings of HSTD-8 2011, in preparation.

[6] ATLAS IBL Collaboration, *Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip*, JINST 7 (2012) P11010.

[7] A. Widmer, P. Franaszek, *A DC-balanced, partitioned-block, 8B/10B transmission code*, IBM J. Res. Dev. 27 (5) (1983) 440-451.

[8] M. Barbero et al., *Submission of the first full scale prototype chip for upgraded ATLAS pixel detector at LHC, FE-I4A*, Nucl. Instr. Meth. A 650 (2011) 111.

[9] M. Barbero et al., *FE-I4 pixel readout chip and IBL module*, PoS (Vertex 2011) 038.

[10] L Gonella et al., *The shunt-LDO regulator to power the upgraded ATLAS pixel detector*, JINST 7 (2012) C01034.

[11] M. Mohsine et al., *Design and measurements of SEU tolerant latches*, CERN-2008-008.

[12] M. Mohsine et al., *SEU tolerant latches design for the ATLAS pixel readout chip*, proceedings of TWEPP 2012, in preparation.