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The development of the multi PPD readout electronics with EASIROC and SiTCP

R. Honda[*†], **K. Miwa**

Tohoku University

I. Nakamura, M. Tanaka, K. Yoshimura

KEK

T. Uchida, M. Ikeno

KEK, Open-It

We are developing a new tracking device with scintillating fibers and Multi Pixel Photon Counter (MPPC) for the J-PARC E40 experiment. Since the total number of the MPPC channels is about 5,000, the electronics for the multi-MPPC readout is essential. In E40, two types of fiber trackers will be installed. The electronics is required to have functions such as ADC, multi-hit TDC (MHTDC), which allows to detect both transition edges, and trigger output. We select a special ASIC, EASIROC developed by Omega/IN2P3 in France, as a front-end part of the readout. EASIROC has many functions such as amplifier, shaper, discriminator and bias adjustment for each MPPC. Multiplexed analog output and individual discriminator output are available. We developed an evaluation board with EASIROC and made performance evaluations. The signal to noise ratio obtained by a charge measurement was about 6.3 for the 1 p.e. (160 fC). The inclusive timing jitter of this readout board was about 270 ps (σ). In addition to these functions, MHTDC was implemented in a FPGA on the board. The best case achievable timing resolution of MHTDC was 460 ps (rms). The requirements for the electronics are satisfied and sufficient performance is achieved.

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[*]Speaker.
[†]E-mail : honda@lambda.phys.tohoku.ac.jp

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1. Introduction

We plan to perform an experiment on Σp scattering as J-PARC E40[1]. For E40, two types of detectors consisting of scintillation fibers and Multi Pixel Photon Counter (MPPC) are under development. The image of reaction, detectors and data acquisition (DAQ) system of the E40 experiment are shown in Fig.1. Some detectors such as timing counters and wire chambers are not drawn in Fig.1. The π beam is analyzed by the K1.8 beam line spectrometer consisting of QQDQQ magnets, tracking detectors and timing counters. The momentum of scattered K is analyzed by Superconducting Kaon Spectrometer (SKS) which is located after the target. One of the new detectors for E40 is a cylindrical fiber tracker (CFT) surrounding a liquid hydrogen target to detect scattered proton via Σp scattering. To measure the energy deposit in the fiber and the timing information, ADC and TDC are required for the readout electronics. In addition, trigger output from CFT is also needed to send signal to the level 2 trigger to reduce the trigger rate. The other is a beam line fiber tracker (BFT) installed at the most upstream part of the K1.8 beam line spectrometer. We need multi-hit TDC (MHTDC), because BFT has to distinguish the triggered beam particle from accidental backgrounds with a timing information under high rate condition up to 10 MHz. As shown in Fig.1, our DAQ system is based on the network (TCP/IP). Management of network is done by SiTCP[2] which is an implementation of TCP/IP on FPGA. Since all electronic circuits to manage TCP are implemented in FPGA, only FPGA is needed to use the data transfer via network.

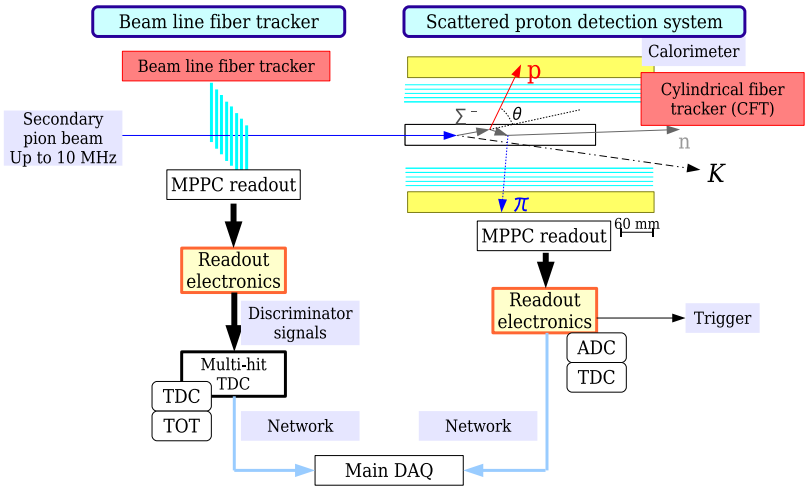

Figure 1: Experimental setup of J-PARC E40.

2. Front-end ASIC

The front-end ASIC is essential to deal with multi-MPPC with one board. We adopted an ASIC named Extended Analogue SiPM ReadOut Chip (EASIROC) developed by Omega/IN2P3 in France[3]. EASIROC has 32 MPPC inputs and all essential functions to operate many MPPCs such as amplifier, discriminator and bias adjustment for MPPCs. The schematic of one channel

in EASIROC is shown in Fig.2. We can adjust the gain of MPPC channel by channel by varying bias voltage by using the input DAC with 20 mV step. There are two amplifier parts in EASIROC, so-called high gain (HG) and low gain (LG) with a factor 10 between the two. The slow and fast shapers shape the amplified signal for the measurement of charge and timing, respectively. The capacitor after the slow shaper stores the voltage corresponding to the signal height. Stored voltage can be read via the read shift register serially in readout period. On the other hand, the discriminated signal is output individually. The bias voltage, the gain of amplifier and the voltage threshold for discriminators are programmable.

3. The evaluation board

We made an evaluation board with EASIROC and SiTCP to make performance evaluation. As shown in Fig.3, the board has one EASIROC and two ADCs (AD9220) for high gain and low gain. The network functions are managed by a small card to use SiTCP, so-called SOY board. The configuration of EASIROC and data taking are done by FPGA on the board.n We can communicate with FPGA via network through SiTCP. The SiTCP can be implemented into FPGA on the board, however, we separated the SiTCP part from the evaluation board for the performance evaluation. The board has four logic inputs and four logic outputs connected to FPGA, which can be utilized as trigger I/O. The individual discriminator outputs from EASIROC are connected to the FPGA directly. Each discriminator signal is applied for various purposes such as input of the MHTDC, making matrix trigger or direct output with LVDS standard.

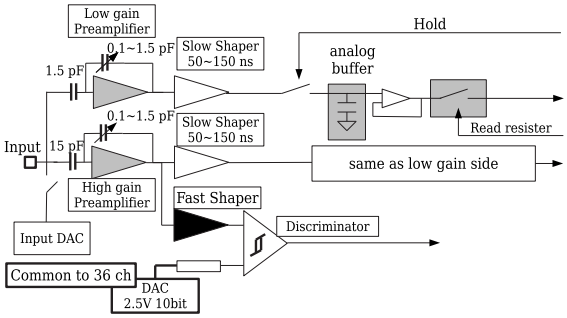

Figure 2: The Schematic of one channel in EASIROC.

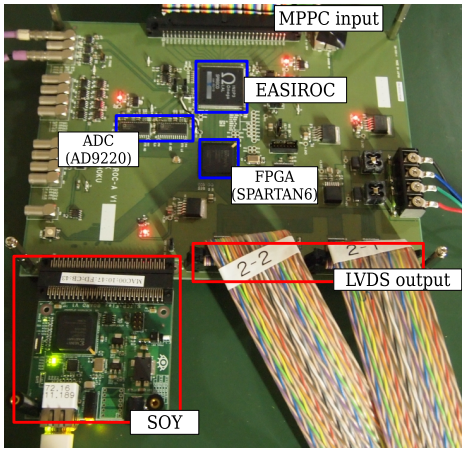

Figure 3: Picture of the evaluation board.

3.1 Signal to noise ratio for the charge measurement

The signal to noise ratio (SNR) for the charge measurement of the evaluation board is obtained by measuring the pedestal and the signal while injecting a fixed input charge. The charge corresponding to 1 p.e. is 160 fC, assuming the gain of MPPC is 10^6. We took data for the injected charge by changing the amount of charge from 160 fC to 1600 fC by an attenuator. Fig.4 shows the result for the high gain side. The leftmost peak is the pedestal and others show the voltage

corresponding to 1 p.e., 2 p.e. and so on. The SNR is defined as following,

$$SNR = 20\log_{10}(gain/noise(\sigma)), \tag{3.1}$$

where, the *gain* is the difference between the pedestal and the peak corresponding to 1 p.e. and the *noise* (σ) is a standard deviation of the pedestal. The obtained SNR for 160 fC is about 6.3. The gain for 1 p.e. for each products of HAMAMATSU, C10507-11-100, C10507-11-050 and C10570-11-025[4], are 2.4×10^6, 0.75×10^6 and 0.275×10^6, respectively. The performance of the charge measurement is satisfactory for the E40 requirement.

3.2 Timing jitter

The timing resolution of the detector system is also an important issue. Since the background ratio due to the accidental coincidence on BFT, which is installed in the beam line, must be less than 0.05 for E40, the timing resolution of BFT is required to be better than 0.8 ns (σ). EASIROC, FPGA and others can cause a timing jitter due to various factors. We have to know the timing jitter of our electronics.

The timing jitter was also measured by injecting a charge. A charge generated by the clock source was used as an input for EASIROC. The time difference between discriminator output and the delayed clock signal was measured by using an external TDC, CAEN v775. The discriminated signal is output from a logic output on the board to measure the time by CAEN v775. The injected charge was attenuated to 160 fC for this measurement. The voltage threshold of the EASIROC discriminator was set to 0.5 p.e.. The obtained time distribution is shown in Fig.5. The TDC one channel corresponds to 190 ps in Fig.5. The standard deviation of about 270 ps is obtained by fitting with the Gaussian function. This result includes the jitter from EASIROC, FPGA and the attenuator which was applied to make a small input signal. The obtained result of 270 ps (σ) is not negligible but acceptable.

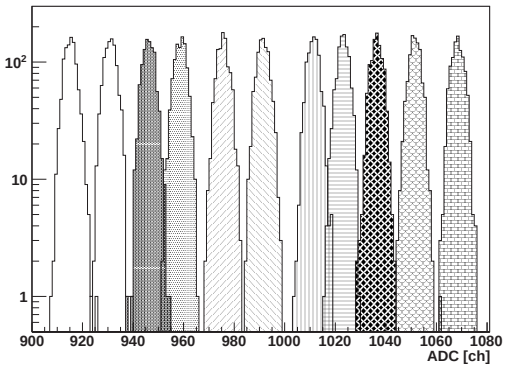

Figure 4: The distribution of ADC obtained by varying an input charge.

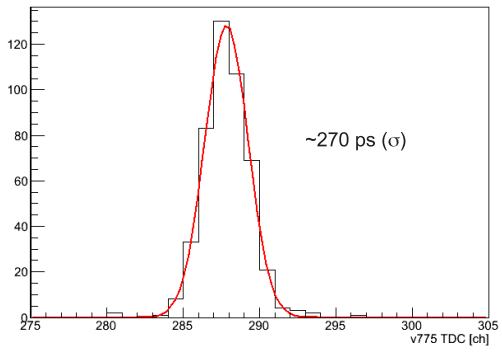

Figure 5: The distribution of TDC obtained by injecting a charge.

3.3 MHTDC in FPGA

We need timing accuracy of 1 ns for MHTDC in FPGA, because the required timing resolution for BFT is 0.8 ns. The MHTDC can be implemented into FPGA with a counter and a fast

clock. However, it is impossible to generate the clock of 1 GHz due to the performance of FPGA. Therefore, four clocks, which phases are shifted by 90 degrees with respect to each other, are used to achieve timing accuracy of 1 ns. The implementation method of MHTDC in FPGA is shown in Fig.6. There are four counters which are driven by the different clocks. The features of MHTDC are shown in Table.1.

Table 1: Features of MHTDC

Time window	Depth	1 ch	Mode
2 μs	8	1 ns	common stop

The performance of MHTDC was evaluated with the same method which was used to measure the timing jitter of this board. The MHTDC measured the time difference between the discriminator output from EASIROC and the delayed clock signal. The obtained distribution of MHTDC by injecting a charge is shown in Fig.7. The root mean square of this distribution is 530 ps (rms). We have to consider the timing jitter which is mentioned in the section 3.2. Assuming the resolution of MHTDC and the timing jitter of the electronics are independent, the timing resolution of MHTDC in FPGA is estimated as 460 ps (rms) by propagation of error.

There is an important requirement for MHTDC, we need charge information to correct the time walk to obtain the required timing resolution for BFT. In ordinary method, the time walk is corrected by measuring both ADC and TDC data. However, the trigger latency for the ADC measurement is not enough for the trigger timing determined by other counters. In addition, BFT has to be operated under a high rate condition up to 10 MHz. It is impossible to measure the correct pulse height due to the pile-up problem under such high rate condition. Therefore, the Time Over Threshold (TOT) is essential for the readout of BFT. Energy can be estimated by measuring the width of the discriminated signal, TOT. The MHTDC in FPGA can measure both transitions of the discriminator signal.

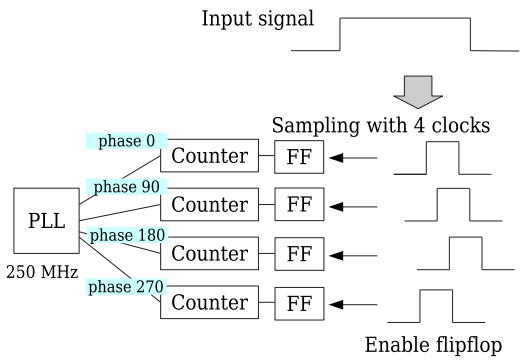

Figure 6: The schematic of MHTDC in FPGA.

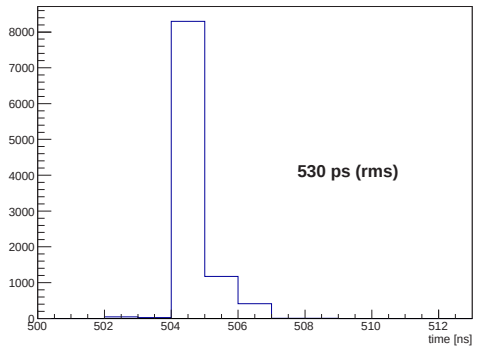

Figure 7: The distribution of MHTDC obtained by injecting a charge.

3.4 Dead time

There are three causes of dead time, that is the conversion times of ADC, TDC and data transfer. Since ADC converts charge of all channels to digital data serially, the conversion time is

constant value of about 60 μs. The dead time of MHTDC depends on the number of hits, however, it is always shorter than the dead time of ADC. Since data acquisition procedures of ADC and MHTDC run parallelly, the dead time of conversion phase is determined by ADC. Therefore, the readout for CFT causes the longest dead time in this readout system, because only CFT requires the application of ADC. The data transfer time depends on the data size, that is, the number of hits in MHTDC. The dead time of 15 μs is expected in the experimental condition for E40. The dead time of readout for CFT is sum of the conversion time of ADC and the data transfer time. Dead time of the readout for CFT is estimated as 75 μs totally. The expected trigger rate in E40 is 3 kHz. The readout dead time for the random trigger will be 20 % with 75 μs dead time for 3 kHz. Expected dead time of 20 % is acceptable for our experiment.

4. Summary

We are developing a new readout electronics for multi-MPPC to readout the scintillation fiber trackers for E40. Because CFT requires to measure the energy deposit and the timing information, the on-board ADC and MHTDC are required for the electronics. The EASIROC chip is suitable for our board, because EASIROC has all essential functions to achieve our requirements. Therefore, an evaluation board with EASIROC was developed. Since our DAQ system is based on the network, SiTCP is adopted as a communication interface. MHTDC was implemented in FPGA by counting four 250 MHz clocks with different phase. The performance evaluation for the charge and timing measurements and MHTDC in FPGA were performed. SNR of the charge measurement for 160 fC was 6.3. The inclusive timing jitter of the readout board was 270 ps. These are sufficient performances for our application. TDC in FPGA worked well as MHTDC which has timing accuracy of 1 ns. The readout board, which can take data of a charge and a timing, was successfully developed.

5. Acknowledgement

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References

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