

Results from the Gigatracker Prototypes: Two Pixel Front-End ASICs with Sub-ns Time Resolution for the NA62 Experiment

Sara Garbolino*

Dip. Fisica Sperimentale e INFN Torino

E-mail: garbolin@to.infn.it

G. Aglieri Rinella^a, V. Carassiti^c, A. Ceccucci^a, E. Cortina^d, J. Daguin^a, G. Dellacasa^b, M. Fiorini^a, P. Jarron^a, J. Kaplon^a, A. Kluge^a, F. Marchetto^a, E. Martin^d, A. Mapelli^{a,f}, G. Mazza^b, M. Morel^a, M. Noy^a, G. Nüsse^d, P. Petagna^a, L. Perktold^a, F. Petrucci^{c,e}, A. Cotta Ramusino^c, P. Riedler^a, A. Rivetti^b, R. Wheadon^b

^aCERN, Geneva Switzerland, ^bINFN Torino, Italy, ^cINFN Ferrara, Italy, ^dUCL Louvain la Neuve, Belgium, ^eUniversity of Ferrara, ^fEPFL Lausanne, Switzerland

The NA62 experiment aims to measure the ultra-rare decay of a kaon into a pion and neutrino-antineutrino pair at the Super-Proton-Synchrotron (SPS) accelerator at CERN. This measurement could provide a decisive test of the Standard Model. The upstream detector, namely the Gigatracker (GTK), will perform the momentum and angular measurements of the incoming beam with sub-ns time resolution in order to provide a tight time coincidence between the kaon and the pion tracks [1, 2]. In order to achieve the required time resolution of 100 ps (rms) it is necessary to compensate for the discriminator time-walk [3]. For this purpose two complementary architectures have been explored. The first one is based on a simple pixel cell, featuring a front-end amplifier followed by a leading-edge discriminator and a transmission line driver and by high precision Time-to-Digital-Converters (TDC) in the end of column shared by a group of pixels [4, 5]. The second option aims to maximize the on-pixel signal processing using a Constant-Fraction-Discriminator (CFD) followed by a TDC on each cell [6, 7, 8]. The two architectures have been designed and produced as small-size prototypes in 130 nm CMOS technology and the ASICs were bump-bonded to 200 μm thick silicon sensors. The recent experimental results obtained from the prototype assemblies during laboratory and beam tests are described in this paper.

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*Speaker.

1. The NA62 experiment

The NA62 experiment will exploit the CERN SPS to probe the very rare kaon decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$. It will use a continuous beam of $8 \cdot 10^8$ part/s having a momentum of 75 GeV/c to have a direct measurement of the branching ratio of this channel. The aim of the experiment is to collect about 80 events having a signal to background ratio of 10% in two years of data taking. Due to its theoretically very clean character this channel is extremely attractive to study the physics of flavour and to make a decisive test of the Standard Model. Furthermore it is highly sensitive to new possible degrees of freedom beyond the Standard Model.

The experiment basically consists of two spectrometers, one for the beam and one for the decay products in the forward direction, where particle identification, momentum measurement and photon vetoing are used with a certain degree of redundancy in order to suppress background. The detector that will perform the momentum and angular measurements of the incoming particles and provide the timing information is the GTK. It consists of three stations of hybrid silicon pixel detector, each formed by a single sensor covering an area of 60 mm x 27 mm and 200 μm thick. Each sensor will generate single-ended signals which will be read-out by ten front-end chips bump-bonded to them.

2. GTK timing requirements

While the momentum measurement is not a critical issue, to reach the 100 ps (rms) time resolution on the track the particle should be detected with a resolution better than 200 ps (rms) on the single hit. While considering this specification, one should take into account the timing errors due to the jitter induced by noise, to non-linearities introduced in digitization and to the time-walk deriving from statistical fluctuation in the total charge released by the particle in the sensor. Concerning the last point, a preamplifier is usually designed in order to respond to different input charges with signals having the same shape but different amplitudes. This means that signals with higher amplitude will cross the discriminator threshold sooner than lower ones.

Given its systematic nature, time-walk can be compensated off-line by recording the amplitude of the signal in parallel to the time. In the Time-over-Threshold (ToT) technique the amplitude information is obtained by tagging the times at which the leading and the trailing edges of the discriminator pulse cross the threshold. This double measurement increases the amount of data to be transmitted. Furthermore, to get the target timing accuracy, a very precise calibration of the time-walk vs ToT curve must be performed on a pixel by pixel basis.

As a different approach one can use a self-compensation scheme, such as a CFD. It works by comparing a delayed copy of the signal with an attenuated one generating a bipolar signal with a zero crossing time independent from the signal amplitude. The use of an on-line compensation implies a more complex architecture and a higher space occupation and power consumption.

3. Two complementary architectures

The final ASIC will contain 1800 independent channels organized in a matrix of 45 rows per 40 columns of pixels covering an area of 300 μm x 300 μm . In order to understand which solution

has more appropriate performances for this application, two different architectures have been explored. The first one is based on off-line correction of data and on a minimal pixel cell, each formed by a transimpedance preamplifier followed by a leading-edge discriminator (see Fig. 1(A)). The discriminator output is sent downstream to the end of column where it is used to latch into local registers a time code for the rising and falling edges provided by a Delay-Locked-Loop (DLL) based TDC.

The second architecture (see Fig. 1(B)) follows a complementary and more ambitious approach

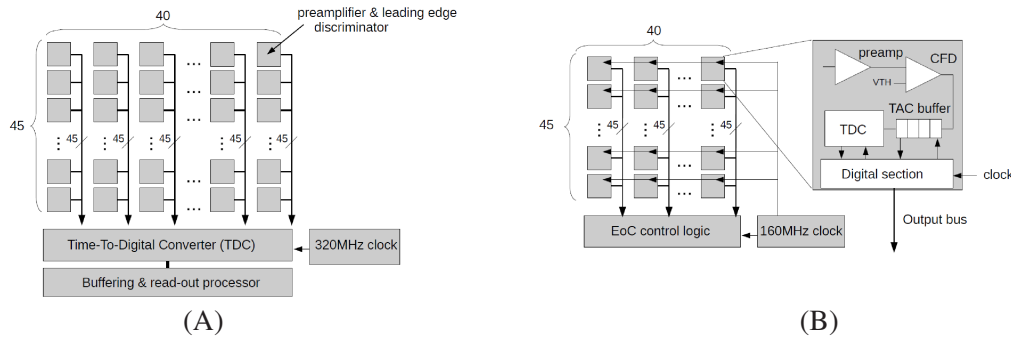


Figure 1: (A) End-of-Column and (B) TDC-per-Pixel architectures

trying to exploit the relatively big area of the pixel to perform already at pixel level all signal processing, including time-walk compensation and time to digital conversion. Each channel contains a transimpedance preamplifier followed by a CFD and by a Wilkinson ADC based TDC. Prototypes of the two solutions have been designed and produced in 2009 and bump-bonded and tested in 2010.

4. End-of-Column (EoC) Demonstrator

The EoC demonstrator makes use of the ToT technique described above. It consists of a single folded column of 45 cells surrounded by test pixels. The analog front-end fills half of the pixel area, while the other half is used to transmit the output of the pixels to the end of column.

4.1 Laser test

The time resolution was first measured using an infra-red laser injecting the charge at the center of the pixels. The result is about 70 ps (rms) at 2.4 fC (see Fig. 2). The EoC prototype has shown excellent performances at the laser test bench. The concept of transmitting out of the pixel precise timing signals with an integrated transmission line was confirmed. No particular issue with digital noise pick-up has been found with this circuit.

4.2 Beam test

In the beam test of the EoC four different stations were used. The resolution obtained was 175 ps (rms), as shown in Fig. 3. The deterioration of the resolution was mostly due to two phenomena, on one hand by the non uniform geometry of the electrical field in the pixel (Fig. 4(A) and 5) and on the other hand by the variations in the charge released by the particle along the sensor (Fig.

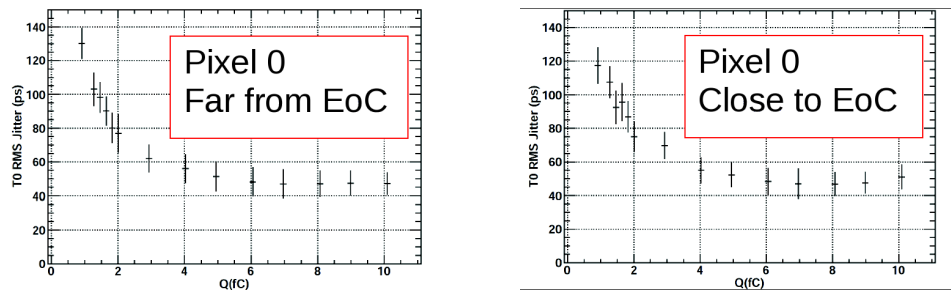


Figure 2: Time resolution measured for laser charge injection at the pixel center results in 70 ps (rms) at 2.4 fC

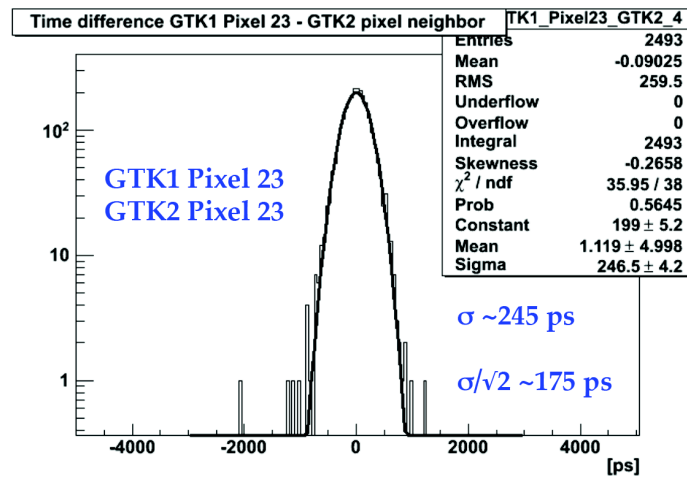


Figure 3: Time distribution measured on two pixels of two boards at the beam test. The resulting time resolution is 175 ps (rms)

4(B)) which both cause a shape variation of the input signals. It is clear that every architecture is affected by this phenomena, however the CFD should be less sensitive to shape variations than the ToT. A resolution of 175 ps still matches the target value, albeit with a relatively small safety margin. The time resolution is limited by intrinsic signal fluctuations in the sensor rather than by the performance of the front-end electronics. Therefore, to improve the timing figure of this architecture, one should work mostly on the sensors properties (e.g further increasing the electric field, using a faster sensor, etc...).

5. TDC-per-Pixel Demonstrator

The TDC-per-Pixel demonstrator is formed by a matrix of three columns, a short one of 15 cells and two folded columns of 45 cells. It also contains two spared pixels for analog testing. Each cell contains a digital and an analog part physically separated and most of analog area is filled by the TDC and by the CFD filter. Due to amount of logic in the pixel, the substrate noise is a critical issue. A very interesting shielding option, consisting in embedding the full digital logic in a dedicated well, has been later introduced in the process, but was unfortunately not yet available at the time of the design.

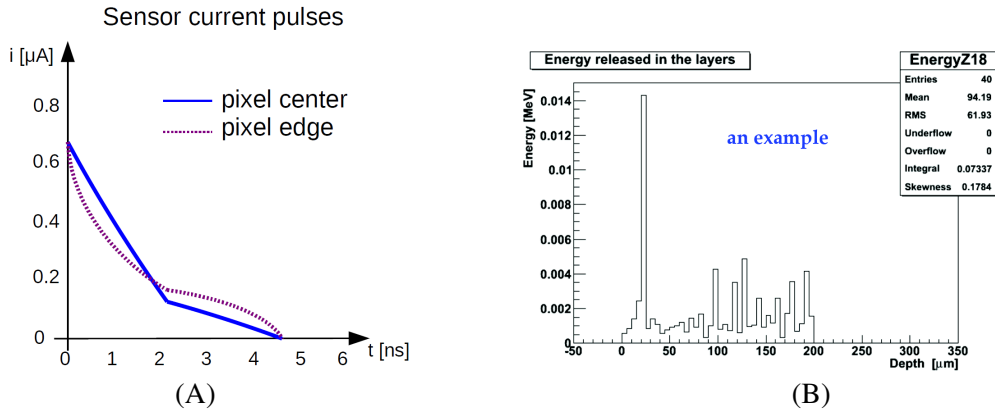


Figure 4: (A) Contribution to timing error coming from signal shape variations due to border effects and (B) to charge straggling

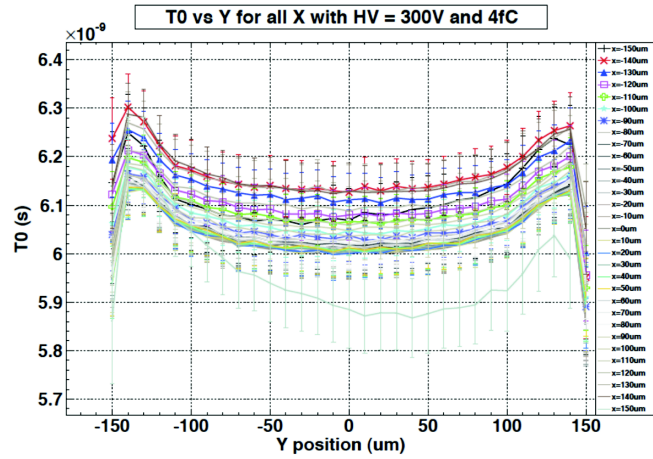


Figure 5: A complete pixel area scan performed with the laser highlights the border effect contribution to timing error

5.1 TDC linearity

The linearity of the TDC has been measured for all the pixels in the matrix. It is possible to test the TDC separately from the analog chain by sending test pulses directly to its input. Sending a set of 10^6 pulses with random phases with respect to the clock, the probability of each code would be, in an ideal 7-bit TDC, $N_{th} = \frac{10^6}{2^7}$. The experimental number of counts differs from this value because of non-linearities. The Differential Non-Linearity (DNL) assesses the deviation of each bin from the ideal bin width, while the Integral Non-Linearity (INL) describes the maximum error between the expected code and the actual one. A DNL and an INL respectively lower in modulus than 0.5 and 1 ensure that there's no missing code.

$$-0.5 < \text{DNL}(i) = \frac{N_{\text{exp}}(i) - N_{\text{th}}(i)}{N_{\text{th}}(i)} < 0.5 \quad (5.1)$$

$$-1 < \text{INL}(k) = \sum_{i=0}^k \text{DNL}(i) < 1 \quad (5.2)$$

A typical result shows a good linearity since there's no missing code in the histogram (Fig. 6) and the DNL and INL calculated for all the pixels in the matrix don't exceed the mentioned values (see Fig. 7).

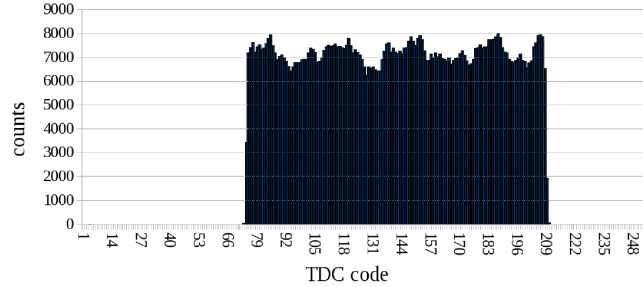


Figure 6: Typical TDC output when hit by a set of Test Pulses with random phases with respect to the clock

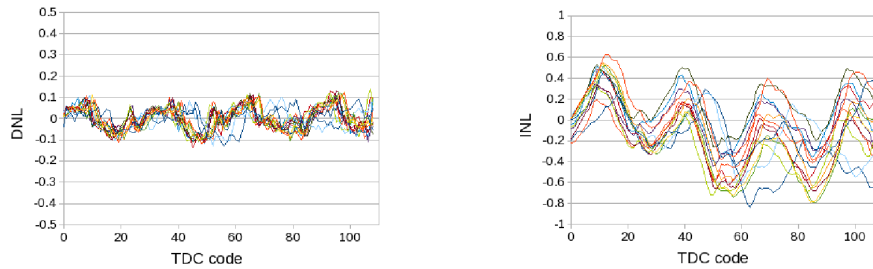


Figure 7: DNL and INL measured for all the matrix pixels indicating a good linearity

5.2 Jitter

For what concerns the jitter, it has been measured sending 10^3 synchronous signals and moving their phase with respect to the clock in steps of 20 ps in order to explore the whole TDC bin width, as shown in Fig 8. For each bin a count distribution is obtained, which rms is the convolution of the jitter with the TDC quantization noise. This operation has been repeated for a set of charges of interest resulting in a jitter lower than 100 ps (rms) at 2.4 fC.

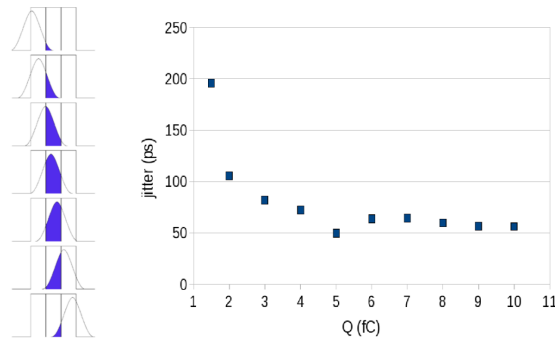


Figure 8: Typical jitter measured from a pixel in the matrix

5.3 Time-walk

The time-walk was first measured at the oscilloscope, directly at the analog output of the CFD in test pixels with the clock switched-off. From the convolution of the time-walk curve with the expected Landau for the experiment (see Fig. 9), the time-walk contribution to time resolution resulted in 92 ps (rms). The same quantity measured for the matrix pixels from the end of column

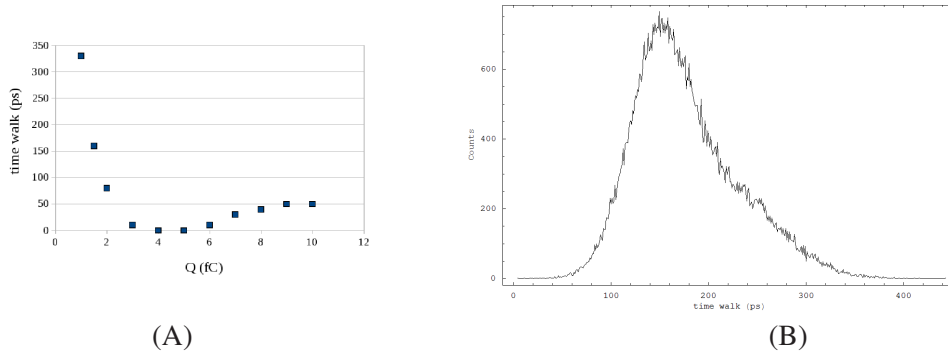


Figure 9: (A) Time walk measured with the clock switched-off. (B) The convolution with the Landau of the experiment gives 92 ps (rms)

with the full processing chain active has shown an average time-walk higher than 500 ps (rms). The deteriorated resolution measured when the digital part is active is due to modulations on the

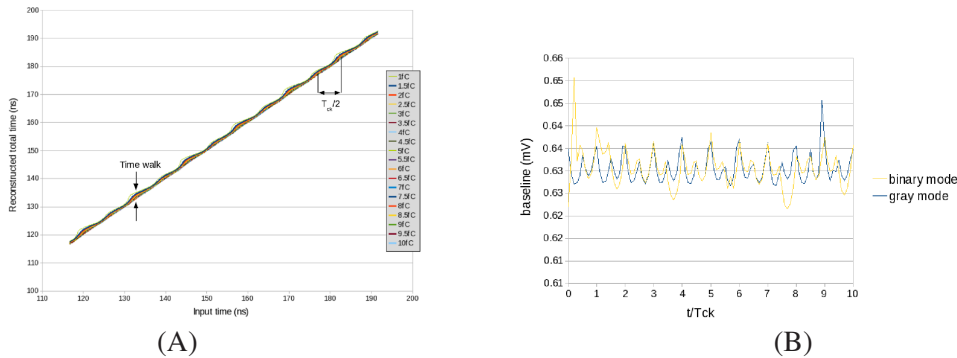


Figure 10: (A) A Test Pulse delay scan has been performed. The total output times vs hit times were reconstructed for charges from 1 fC to 10 fC. The spread of the curves represents the time-walk. Each hill corresponds to a clock transition, while the ideal curve would be a straight line. (B) Bounce of the baseline at the output of the CFD. The disturb is synchronous to the clock

baseline that corrupt the shape of the CFD bipolar signal (see Fig. 10(A)). A detailed analysis has shown that this modulation is synchronous to the clock (Fig. 10(B)). The interference is mostly due to the digital drivers that propagate the clock and the counter signals towards the pixel matrix. For a future version, the drivers will be insulated embedding them in a dedicated digital well. Furthermore an improved design of the amplifier which makes it less sensitive to the digital noise pick-up has also been developed.

6. Summary and Outlook

Two ASICs implementing two complementary architectures have been designed and produced

in the R&D of the GTK for NA62 experiment. The first solution is based on a simple and almost all analog pixel and on off-line correction of time-walk. The complete separation between the digital and analog part, which allows also to avoid strong digital drivers, was crucial to minimize the digital noise pick-up and resulted in excellent performances at the electrical test. An overall resolution of 175 ps (rms) was measured in the beam test. This value is still adequate for the purpose of the NA62 experiment, but is relatively close to the upper limit of 200 ps (rms). The challenge will then be in preserving the good performance measured with the prototype at the full system level.

All the blocks in the TDC per pixel architecture were functional, but the on-chip digital noise limited the global timing performance to 500 ps (rms). In principle a CFD based approach could be more resilient to the effect deriving from statistical shape variation, provided that the delay and the fraction of the CFD network are properly chosen. Additionally it could reduce significantly the burden of the calibrations.

For these reasons and for the contingency of the experiment a full-size version of the EoC is now in preparation and will serve as the baseline solution for the experiment. An improved version of the CFD based architecture will also be submitted and could be used in the future if its potentials will be confirmed by the experimental measurements.

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