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CMS Silicon Tracker upgrade for HL-LHC

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LHC is expected to increase its luminosity above the original nominal value of $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, eventually achieving $5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ after major upgrades will be performed after 2020. This configuration of the machine is known as High Luminosity-LHC (HL-LHC).
CMS needs a completely new tracking system to maintain adequate performance in the HL-LHC environment and to provide tracking information for the Level-1 trigger decision.
The most relevant requirements and constraints are summarized, along with highlights from some of the R&D activities.

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	LHC		HL-LHC	
	current (12/2011)	nominal	low pile-up	high pile-up
peak luminosity [$cm^{-2}\,s^{-1}$]	3.6×10^{33}	1×10^{34}	5×10^{34}	5×10^{34}
integrated luminosity [fb^{-1}]	~ 5.7	500	3000	3000
number of bunches per ring	1380	2808	~ 2800	~ 1400
c.m. energy [TeV]	7	14	14	14
bunch crossing interval [ns]	50	25	25	50
number of pp events / crossing	~ 15	~ 20	~ 100	~ 200
number of charged particles in Tracker	~ 500	~ 1000	~ 5000	$\sim 10\,000$

Table 1: Some parameters of the LHC and the HL-LHC

1. The current CMS Silicon Strip Tracker

The inner Tracker of the CMS detector [1] at the LHC is completely based on silicon sensor technology. The Tracker is placed inside a large solenoid providing a magnetic field of 3.8 T. The CMS coordinate system is defined such that the z axis coincides with the nominal beam line. The radial distance from the z axis is denoted as r. The polar angle θ is measured from the positive z axis and the azimuthal angle φ is measured in the plane perpendicular to it. Pseudorapidity η is defined as $\eta = -\ln\left[\tan\left(\frac{\theta}{2}\right)\right]$.

The CMS Silicon Strip Tracker is the largest detector of its kind ever built and operated. It is roughly 5.6 m long in the z direction, with a diameter of 2.2 m. With its 10 barrel layers and 12 end-cap disks per side, it features about 200 m^2 of sensitive surface in 15 148 modules with 9.3×10^6 channels read out through 36 392 analogue optical links.

The present Tracker was designed to operate at luminosities up to about $1\times10^{34}\,cm^{-2}s^{-1}$. Significant robustness and redundancy in the tracking capability was implemented in the detector layout, to ensure optimal performance for several years of operation (up to an integrated luminosity of about 500 fb^{-1}), with basically no maintenance or repairs.

2. The LHC upgrades

The Large Hadron Collider (LHC) project is currently[1] in its first phase of physics exploitation with a centre-of-mass collision energy of 7 TeV (half of the nominal value) and a record peak instantaneous luminosity of $3.304\times10^{33}\,cm^{-2}\,s^{-1}$ (one third of the nominal value). The performance of the LHC in delivering luminosity to the experiments is continuously growing.

According to the machine plans the nominal luminosity of $10^{34}\,cm^{-2}\,s^{-1}$ and centre-of-mass energy of 14 TeV should be reached after a machine upgrade, which will be performed during the first long shutdown of the LHC planned to take place in 2013-2014.

Two more long shutdowns are planned for the mid 2010s and early 2020s and the instantaneous luminosity of the machine should exceed the design goal. Before the third long shutdown the silicon pixel vertex detector of CMS will be replaced to cope with the increased particle density. This operation is known as Phase 1 upgrade and it is not covered in the present article.

[1] as of December 2011

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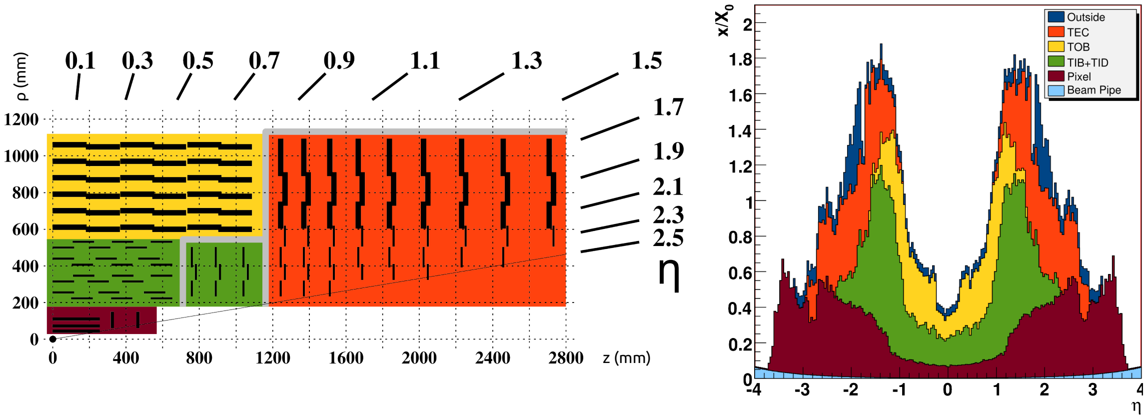

Figure 1: Sketch of the Silicon Strip Tracker layout (left), and distribution of material in radiation lengths as a function of pseudorapidity (right). The peaks in the regions $1 < |\eta| < 2$ contain contribution from the services routed between barrel and end-cap.

After the last upgrade of LHC the instantaneous luminosity is expected to reach $5 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$. This scenario is known as High-Luminosity LHC (HL-LHC, see Table 1).

The HL-LHC scenario represents a challenge for the detectors due to the high radiation dose (up to $10^{15}\,\mathrm{n_{eq}cm^{-2}}$ at 20 cm) and the high number of pile-up events (100 to 200). For the CMS detector, these high levels of pile-up are a problem for event reconstruction (separating the signal of different particles and reconstructing primary events). Under these conditions the Silicon Strip Tracker must be replaced during the third long shutdown in preparation of HL-LHC (Phase 2 upgrade).

3. Phase 2 upgrade

The phase 2 upgrade gives the collaboration the opportunity to improve the performance of the detector: increasing the resolution of the track reconstruction and possibly reducing the amount of particle interactions in the tracking volume.

The material in the current CMS detector ranges from approximately 50% of a radiation length in the barrel section to 180% at $|\eta| = 1.5$ (Figure 1). This is not only detrimental to the resolution of the electromagnetic calorimeter, but affects also the tracking resolution of charged particles through multiple scattering. For example the resolution of muons with p_T up to about $10\,\mathrm{GeV/c}$ is dominated by this.

The granularity of the detector should increase approximately by a factor 5 in order to cope with a maximum foreseen pile-up of 200 collisions per bunch crossing and to keep the occupancy to a few % level as in the current detector.

The radiation hardness of the sensor material should increase to move from the current LHC design integrated luminosity of $500\,\mathrm{fb^{-1}}$ to an expected $3000\,\mathrm{fb^{-1}}$ for HL-LHC.

To this date the only sub-detector to be fully replaced in CMS for HL-LHC is expected to be the Tracker. On the other hand the services for the tracker (readout, power supply, cooling, etc.) are not accessible without partially dismantling those for other sub-detectors. For this reason the upgraded Tracker is constrained to using the same services as the present one.

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This fact together with the request for an increased granularity drove the choice of technologies for readout, powering and cooling. A digital readout is required to pack more data in the same available band-width. Power should be delivered at a higher voltage to reduce ohmic losses in the services and then converted to the required low voltage inside the tracking volume. Finally a CO_2 evaporative cooling is foreseen, which allows to deliver more cooling power through the same pipe section.

The combinatorial background poses also problems to the Level-1 trigger of the experiment, presently based on calorimeters and muon detectors, making it impossible to keep the trigger rate within the nominal range (around 100 kHz) while applying reasonable thresholds to the trigger variables. The CMS collaboration plans to improve the trigger, for example by installing a fourth layer of the Cathode Strip Chambers muon detector and re-designing the Level-1 trigger hardware. Nevertheless these improvements will be insufficient for the HL-LHC luminosity.

A large event rate reduction factor is currently achieved in the High-Level software Trigger by using information from the Tracker. Including this information in the Level-1 processing would allow a much better rejection of combinatorial background [2, 3].

The collaboration is therefore studying the option of sending tracking information in real time to the Level-1 trigger.

4. Sensor R&D

Reducing the strip length (from 10 cm to 2.5 cm in the inner layers) and pitch (to 90 µm in all the detector) provides the needed detector granularity

The dark current induced by radiation damage must be kept below the critical threshold for thermal runaway in order for the detectors to be operational. This will be achieved not only through the cooling system, but also by designing sensors with relatively low full depletion voltage and using thinner wafers with respect to the current ones, which range from 300 to 500 µm.

The collaboration started a vast measurement campaign [4] to qualify the sensor technology suitable for the upgrade. A dedicated batch of sensors on 6-inch wafers was produced by Hamamatsu Photonics KK with different substrate, thickness, implants and geometries.

Three different technologies for the substrate production are investigated, with different active thicknesses: Float-zone (120, 200, 300 µm), Magnetic Czochralski (120 µm) and epitaxial (50, 100 µm). For each substrate technology wafers were produced with three doping types (n-type bulk, p-type bulk with p-spray or p-stop isolation). Each wafer contains many test structures used in different tests. The diodes (7×7 mm^2) are used to characterise the material through electric measurements (IV- and CV-curves).

Multi-geometry strip detectors are the largest structures (roughly 3×6 cm^2) with 3 cm-long strips arranged in groups of 32 strips with different pitches from 70 µm to 240 µm. This kind of sensors could be used in the inner region of the Phase 2 strip Tracker. A new kind of structure is also investigated: arrays of long pixels (approximately 1 mm long). These could be read out by a pixel-like bump-bonded chip and used to directly measure the track z coordinate.

Many other structures were designed on this wafer and are currently tested: new pixel (with a footprint compatible to the current pixel Read-Out Chip), a sensor with an on-wafer pitch-adaptor,

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a sensor dedicated to the measurement of the Lorentz angle, some structures to monitor the production and other smaller test structures.

5. Front-end electronics

The available readout bandwidth is constrained by the number of optical fibres already in place and by power consumption on the transmitters. This fact, together with the foreseen fivefold increase in detector granularity, drove the system design towards a simplified strip signal readout scheme. Therefore analog readout was dropped in favour of a binary readout in the design of the front-end chip. As a drawback no measurement of the energy loss will be available and the hit resolution cannot be improved using the charge sharing between neighbour strips.

The CMS Binary Chip (CBC) is a 130 nm CMOS front-end chip designed for the Phase 2 CMS Tracker upgrade. It has 128 channels, it is designed to read out signals of either polarity from short strips (capacitance up to 10 pF) and can sink or source sensor leakage currents up to 1 µA. Each input channel has a 256 cells deep pipeline (corresponding to 6.4 µs). The first prototypes were already produced and the first evaluations showed [5] for a typical load capacitance of 5 pF a good noise performance (820 e^-) and power consumption (< 0.3 mW/channel), in line with the design.

A Gigabit Bidirectional Trigger and Data Link (GBT) is being developed for the HL-LHC detector upgrades in 90 nm CMOS technology. It is designed to provide a bandwidth of 4.8 Gb/s on an optical line, merging about 10 parallel electrical input lines, with a power consumption of 2.1 W [6, 7]. The CMS collaboration is interested in the possibility of adapting this chip to a lighter version in 65 nm CMOS, with a single electrical input line, a power consumption reduced to about 500 mW (i.e. roughly 0.25 mW/channel) and a similar bandwidth. This would allow to integrate the transmitter directly on the modules, simplifying the system design and integration. The CMS Tracker would benefit from the large number of existing optical connections to the counting room, the bi-directional link would simplify calibration and maintenance operations, compared to the present system with separate control and readout links, and the available bandwidth would allow to transmit both Level-1 trigger data for each bunch crossing and the complete event data upon the reception of a L1 trigger.

6. Power

Even taking into account the foreseen large decrease of power consumption of front-ends from the present 3 mW per channel to the foreseen 0.5 mW per channel, the total amount of power to be delivered is expected to be higher than the current one ($P_{front-end} = 33$ kW plus $P_{cables} \simeq 20$ kW dissipated in the cables). Moreover, the smaller feature size of the front-end chips requires a smaller power supply voltage (1.2 V for the 130 nm technology). The proposed solution is to deliver power at a higher voltage to the modules (thus reducing the current and power dissipation) and equip these with DC/DC converters.

A dedicated chip was designed for this and several prototypes in the AMIS technology were produced and tested [8]. Results show that this powering scheme could be used for the Phase 2 upgrade.

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Radiation damage plays an important role in the power management: in order to control power dissipation in the sensors due to the dark current, temperatures below $-10\,^{\circ}$C will be required. Reaching lower working temperature requires a higher cooling power to be delivered with the same external services as the present ones. An attractive solution is a two-phase cooling, exploiting the latent heat of evaporation of the cooling fluid. Also increasing the coolant flux allows designing smaller (and lighter) cooling pipes and to do this in the presence of a gaseous phase of the fluid one needs a high pressure. This lead to the choice of CO_2 as coolant, which boils at 20 bar at $-20\,^{\circ}$C.

The increase in pressure does not need to be compensated by proportionally thicker walls of the cooling pipes, as the current ones are already largely redundant. This will allow to reach an operating temperature of $-20\,^{\circ}$C while reducing the material budget with respect to the present C_6F_{14}-based cooling system [9–11].

7. Tracking in the trigger

In order to transmit tracking information to the trigger processor, the amount of data to be shipped needs to be reduced. This could be achieved by directly measuring p_T on the module and filtering out the low p_T hits ($p_T < 1\,\mathrm{GeV/c}$ to $2\,\mathrm{GeV/c}$). This could be done in CMS thanks to the 4 T magnetic field, by instrumenting each detector module with a pair of closely spaced sensors, as described below.

7.1 pT-2S module

In this module (Figure 2 left) the strips of the two sensors are parallel to each other and the front-end electronics must read out the two sensors at the same time and perform a hit correlation. The local x coordinate of the hits measures the charged particle trajectory perpendicular to the solenoidal magnetic field B, and thus the distance Δx between matching hits in the two sensors is a function of the particle p_T and is different for barrel and end-cap modules:

$$(\Delta x)_{BARREL} = \frac{d}{\sqrt{a^2-1}}\ ;\quad (\Delta x)_{ENDCAP} = \frac{d}{\sqrt{a^2-1}}\frac{r}{z}\ ;\quad a = \frac{2p_T}{0.3\,B\,r}\frac{\mathrm{T\,m}}{\mathrm{GeV/c}} \tag{7.1}$$

where d is the distance between the two sensors and r, z the cylindrical coordinates of the module. Closely matching hits ($\Delta x < \Delta x_{cut}$) belong to high-$p_T$ tracks and are sent through an integrated GBT to be used in the Level-1 trigger.

To have a good p_T discrimination Δx_{cut} must be much bigger than the strip pitch π, which is typically 100 µm. For the CMS magnetic field B of 3.8 T and a p_T cut at $1\,\mathrm{GeV/c}$, the optimal distance between the sensors in the CMS Tracker region varies between 0.8 mm (barrel, $r > 50$ cm) and 4 mm (end-cap, $r \simeq 25$ cm).

When a trigger is received by the module, the complete information of the event is transferred to the standard DAQ system. In order to read out strips from both sensors the hybrids must be placed at the edge of the module, and this limits the minimum strip length to half of the module size (approximately 5 cm).

For each event, f fake high-p_T hits will be found from the combination of uncorrelated low-p_T hits. If N is the number of strips per sensor and H is the average number of hits per event on each

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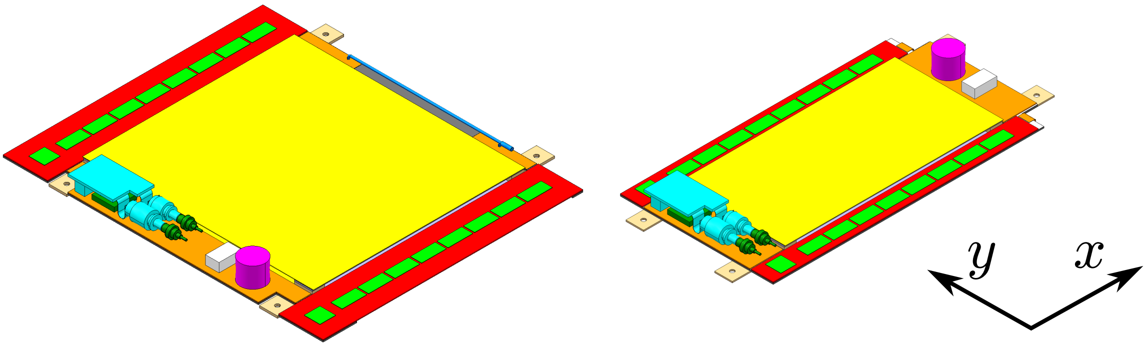

Figure 2: Sketch of module designs, to scale: pT-2S on the left, and pT-PS on the right. Micro-strips are oriented parallel to the sensor edge (from top left to bottom right in this figure). Hybrids are painted in red, sensors in yellow and front-end chips in green.

sensor, $h = H/N$ is called *hit occupancy*, and

$$f = h^2 N \frac{2\Delta x_{cut}}{\pi} \tag{7.2}$$

In order to keep the combinatorial background below 0.1 fake matches per event on a sensor with 1024 strips and a search window of 5 strips, the hit occupancy must be lower than 0.5%. This limits the use of 5 cm-long strips to the region at $r > 50\,\text{cm}$ in the scenario with 100 pile-up events per bunch crossing.

This module measures $r\varphi$ with a precision of $\pi/\sqrt{6}$, but it does not provide a direct measurement of the local y coordinate.

7.2 pT-PS module

In order to overcome the limitations of the pT-2S module, a variant was designed with one of the two sensors being a pixel detector (Figure 2 right). This way the y coordinate of the hit can be measured locally, and is also available for the track reconstruction in the Level-1 Trigger. In this design the hit correlation is integrated in the pixel read-out chip and the connectivity with the strip sensor is implemented through hybrids at the sides of the module. These modules are intended to cover the inner part of the detector, thus a strip length of approximately 2 cm is needed, limiting the size of the sensor to $10\,\text{cm} \times 4\,\text{cm}$. The minimum pixel pitch achievable with standard industrial bump-bonding techniques of 100 μm was chosen for the strips and pixels. The local y measurement precision (380 μm) is determined by the longitudinal size of the pixel (1.3 mm).

7.3 pT-VPS module

A different approach to the construction of a pT module is represented by the Vertically-integrated Pixel-Strip module (or pT-VPS, Figure 3). In this design one 3D chip reads out the pixelated sensor and the short-strip sensor, connected by analogue paths through an interposer, and implements the correlation logic.

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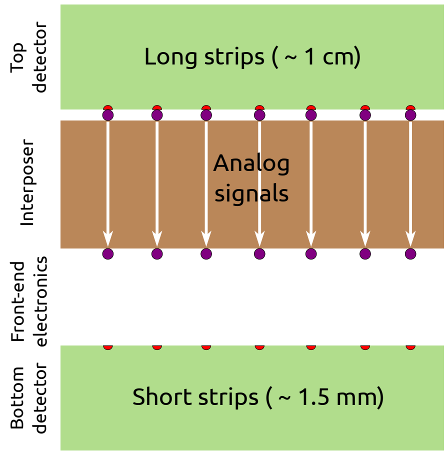

Figure 3: Conceptual schematics of the vertical connections in the pT-VPS module.

The use of vertical connectivity removes all constraints between module dimensions and sensors segmentation. Such a module can in principle be realised in $10 \times 10\,\mathrm{cm}^2$ size, and, if needed, the strip length can be reduced to further reduce the occupancy. Compared to the pT-PS module, the realisation of a module of larger surface offers some advantages for the integration of hermetic surfaces and for the optimisation of the services. On the other hand, the interconnection technologies are challenging: feasibility, reliability and yield for large-surface assemblies need to be verified, also considering the demanding operating conditions inside CMS. In addition, in this concept an interposer covers the entire surface of the module, defining the spacing between the two sensors, providing the top-to-bottom connectivity and carrying at the same time power lines and readout signals: the realization of a lightweight interposer with the needed thickness (about 1 mm) and electrical and mechanical properties is a key issue to realize a module with an acceptable material density.

7.4 Evaluation of Tracker concepts and geometries

In order to evaluate quantitatively different options and geometries for the Tracker upgrade, a standalone software package has been developed (tkLayout) to generate detector layouts starting from a reasonably small set of parameters, and to implement in a simple and flexible way estimates of the material densities for active and inactive volumes, including the routing of the services. The software calculates the expected tracking precision and the performance potential for the L1 track reconstruction, as well as the fraction of converted photons and interacting pions. Besides, it generates summary statistics for the considered layout, such as number of modules, readout channels, active surface, power consumption, estimated total weight, etc. The validation of the package with the modelling of the present Tracker [12] has demonstrated an excellent agreement between the predicted performance and the one measured on the real detector.

A sketch of a layout that was studied in detail [13] is shown in Figure 4 together with an estimate of the corresponding material budget. This layout implements modules with p_T discrimination in the whole tracking volume: pT-2S modules in the outer half of the radial range, and pT-PS modules in the inner half.

This option was shown to allow a more precise tracking with respect to the current detector, presently instrumented with strip sensors. It could also provide data to the L1 decision to reconstruct tracks with a p_T resolution of 2 % to 5 % for $\eta < 2$ and $p_T = 100\,\mathrm{GeV}$, and with a z_0 resolution below 1 mm.

It should be mentioned that the use of modules with pT discrimination in the end-cap configuration is not fully proven, as it may require tuning the spacing between the two sensors according to the (R,z) position, to obtain an adequate discriminating power.

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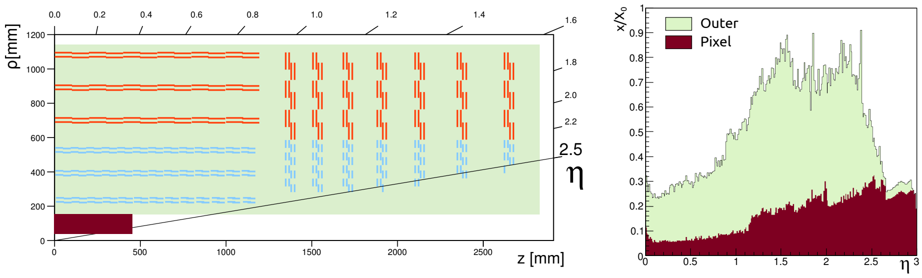

Figure 4: Left: sketch of a possible Silicon Strip Tracker layout for the Phase 2 upgrade: pT-PS modules are drawn in light blue and pT-2S in red. **Right:** distribution of its estimated material in radiation lengths as a function of pseudorapidity.

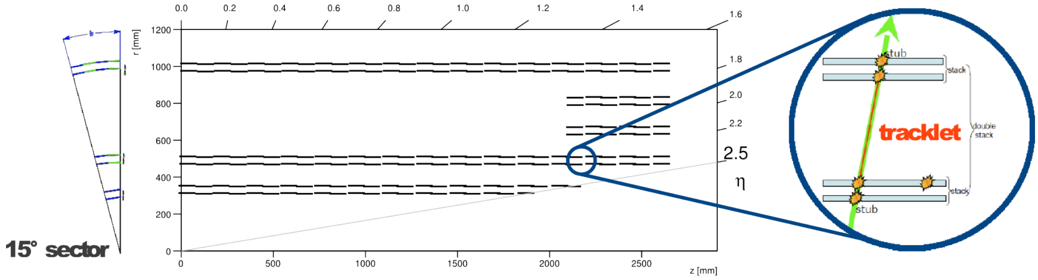

Figure 5: Hierarchical processing of stub coordinates. In a detector geometry where layers are arranged in closely spaced pairs, pairs of stubs are first combined to form "tracklets" which are then used as seeds for the L1 track finding. The modularity in φ is tuned to have self- contained 15° sectors. The concept has been studied in a barrel geometry.

8. Tracking trigger: from stubs to tracks

The coordinates of stubs selected by the pT modules have to be combined in the trigger electronics to form L1 tracks. The goal is to reconstruct with high efficiency the tracks of particles with $p_T > 2\,\text{GeV}$, which should allow to perform isolation cuts on calorimeter clusters. The two concepts considered so far are hierarchical processing in FPGAs and parallel processing in Associative Memories.

The possibility of hierarchically processing the coordinates of the selected stubs in a dedicated set of FPGAs has been studied in some detail, using a detector geometry optimised for trigger reconstruction. Layers are arranged in closely-spaced pairs ("double-stack" geometry) in order to mitigate the combinatorial problem, and pairs of stubs are first combined to form "tracklets" that have sufficient precision to extrapolate to the next double stack (see sketches of Figure 5). Tracklets and remaining un-associated stubs are then combined to form L1 tracks. The geometry is also tuned to have well-defined sectors in the φ view.

Parallel processing in Associative Memories is considered as an alternative approach, which could allow to process stub coordinates in a generic detector geometry, by comparing the collected coordinates with pre-stored patterns, corresponding to the high-pT tracks. This approach was successfully used in the CDF trigger [14], and is been considered for the ATLAS trigger upgrade. However the application in CMS would be of unprecedented size and complexity, and feasibility

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studies have just started.

9. Conclusions

Good progress has been made in identifying options for the implementation of the tracking trigger in the CMS Tracker Upgrade.

The key components of the new detector were identified, the corresponding research lines started and are in the prototyping phase; a large measurement campaign is under way to identify the suitable sensor technology, and the study of options to process the information to form L1 tracks has also started.

Several detector module designs were defined in detail and this allowed to study several detector layouts, also evaluating their expected tracking performance and potential for contribution to the Level-1 trigger.

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