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R&D Progress on The SuperB Silicon Vertex Tracker

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The SuperB asymmetric e^+-e^- collider has been recently approved by the Italian Government. With a design luminosity two orders of magnitude greater than the past B-Factories and by exploiting the low-energy beam polarization, within few years it is expected to start the study of rare B and D meson decays, where New Physics might show up, and lepton flavour violation in tau decays.

Due to the reduced center of mass boost, the vertex resolution must be improved to achieve the same proper-time difference resolution for B decays obtained in BaBar. Thus, based on the layout of the BaBar vertex detector, the SuperB Silicon Vertex Tracker must be equipped with an extra innermost layer (the Layer0), very close to the interaction point. The most stringent physics requirements concern the low material budget and the high-background working conditions of the Layer0: striplets modules, with short strips on high resistivity silicon sensors, are the baseline solution foreseen for the beginning of data taking; an upgrade to pixel sensors, more robust against high background occupancy, is planned at the full luminosity. The latest results on the various pixel options explored by a specific R&D program on different pixel technologies will be described: CMOS MAPS, pixel sensors realized on multiple layers with a vertical integration technology and hybrid pixels.

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1. Introduction: the SuperB project

At the end of 2010 the Italian Government approved the SuperB Factory as the first in a list of flagship national research projects, providing also the funding schedule on a five-year basis. In spring 2011, after a vibration measurement campaign, the site for the accelerator and the laboratory ("The Cabibbo Lab") has been identified in Tor Vergata, near Rome.
An international collaboration took up the challenge of building a new generation e^+-e^- collider, able to deliver a luminosity two orders of magnitude greater with respect to the past B-factories.
The search for effects of New Physics (NP) in the decay of heavy quarks and leptons [1] motivates the need of an integrated luminosity of at least 50-100 ab^{-1}. High statistics is mandatory to reach the sensitivity required not only to discover possible NP effects but also to set constraints on the models describing them.
Furthermore, the SuperB collider is designed to exploit the high polarization of the e^- beam, important for an efficient background rejection in the $\tau^+ \tau^-$ channels; there is also the possibility to switch to lower center of mass energy, at the "charm" threshold, without permanently modifying the optics of the machine.
So far, the so called "Italian approach" (i.e. moderate beam currents, very small emittance and small betatron vertical amplitude at the interaction point) remains as the only viable solution to build the new accelerator, able to deliver a luminosity in excess of $10^{36}cm^{-2}s^{-1}$.
As added value, the crab-waist technique is used to remove dangerous synchrotron-betatron resonances: already tested at DAΦNE, it may allow a further luminosity gain.
The design of such a challenging machine sets indeed a severe constraint on the beam-energy asymmetry: 6.7 GeV positrons collide with the 4.2 GeV electrons beam, obtaining a boost $\beta\gamma$ of 0.24 (to be compared with 0.56 in BaBar). The SuperB detector must cope with this lower center of mass boost by improving the vertex resolution for optimal time-dependent measurements.
Simulation studies have validated the concept a vertex detector based on the BaBar Silicon Vertex Tracker (SVT) layout with the addition of an innermost layer (called Layer0 in the following). It is on this item that most of the efforts of the SuperB-SVT group is focused.
This paper presents several technological options for the Layer0 design. A high resistivity double-sided silicon detector with small strips, called striplets, tilted with respect to the detector's edge, can be the technologically mature choice in the first phase. After two years of running, the luminosity is expected to reach the nominal value and so highly segmented pixel detectors, solutions more robust against high background occupancy, are required. The CMOS Monolithic Active Pixels (MAPS) [2, 3] are a very promising technology but they still require an extensive R&D; the vertical integration offers a technologically leap for pixel detectors but the timescale to reach the process reliability might not match the timeline of the SuperB projects.
Hybrid pixel detectors are a viable and mature option but they must be designed with smaller pitch and thinner than the existing ones.
The SuperB-SVT group is deeply involved in finalizing the R&D activities in view of the next construction phase.

2. The Silicon Vertex Detector Design

The design of the SuperB SVT has been optimized by physics performance studies, taking into account constraints from background considerations. The barrel sections of the 5-layer BaBar SVT [4] have been properly extended to cover an angular acceptance down to 300 mrad in both forward and backward directions and equipped with the Layer0 placed close to the beam-pipe (reduced to a radius of 1 cm and a thickness of about 0.45% X_0).
It is worth saying that in the simulations the parameter driving the sensitivity of the CP time-dependent measurements is the resolution in the proper time difference between the two B mesons, and in a conservative approach we assumed that it should not exceed the value obtained by the BaBar experiment: the absolute vertex precision must be increased by a factor of two.
Setting the resolution on the single hit (z and ϕ) to 10 m and a material budget less than 1% X_0, the Layer0 must be placed at radius of about 1.5 cm, very close to the beam-pipe.
A full Geant4 simulation of the detector and beamline has been used [1] to identify the major sources of background: the main contribution comes from luminosity terms (i.e. irreducible): the $e^+ e^-$ pair production is the most relevant process for the SVT, while radiative Bhabha events are one order of magnitude smaller. Touschek effects have been considered but with proper collimator settings can be kept to a negligible level. The pair-produced leptons have energy in the MeV range. Low transverse momentum tracks are effectively suppressed by the bending effect of the 1.5 Tesla solenoidal magnetic field. Thus the background hit rate deeply depends on radius and for a Layer0 at 1.5 cm the level reaches 20 MHz/cm^2. Concerning the radiation hardness, the equivalent fluence corresponds to 3.7 10^{12} n/cm^2/year and the dose rate to withstand is 3 Mrad/year. In the design of the whole detector the SuperB collaboration decided to set a working safety factor of five on these background estimates.

3. The Front-End chip for strip & striplets

After a survey on the existing front-end chips, we have drawn the conclusion that none of them is matching all the SuperB-SVT requirements: for the inner layers the expected rates are very high (up to about 2 MHz/strip in Layer0) and the shaping time must be kept short (in the range 25-100 ns); instead the long modules of the external layers need shaping time of 0.5-1 s to cope with noise. For dE/dx measurements a pulse height information must be provided.

Two new chips, differing in the analog section, must be designed for the inner and the outer SVT layers. The read-out architecture developed for pixels can be adapted for the strip read-out, matching the stringent requirements on the hit rates up to 2 MHz/cm^2. The studies performed so far didn't produce any evident showstopper that could prevent us from designing of the analog front end and a full VHDL simulation of the chips for the Technical Design Report (TDR). The estimates of the equivalent noise charge (ENC) for each SVT layer, with the chosen peaking time on the $RC^2 - CR$ shaper and the contribution of the analog part to the inefficiency are reported in Fig. 1.

3.1 Striplets

The striplet option for the Layer0 relies on the mature technology of the high resistivity double

Layer	C_D [pF]	available t_p [ns]	selected t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Channel width [μm]	Hit rate/strip [kHz]	Efficiency 1-N
0	11.2	25, 50, 100, 200	25	220	740	3000	1370	0.948
1	26.7		100	460	940		429	0.959
2	31.2		100	590	1100		268	0.976
3	34.4		200	410	940		105	0.982
4	52.6	400, 600, 800, 1000 (or 500 and 1000)	500	490	1000	9000	17.5	0.993
			600	440	940			-
5	67.5		800	560	1090		11.3	-
			1000	500	1030			0.990

Figure 1: Main parameters of the analog section of the SVT strip readout chips for the different layers.

sided silicon detector. On 200 m-thick substrates, short strips (striplets) oriented at 45 degrees with respect to the the edge imply very low material in the sensitive region, less than 0.5 % X_0. Assuming a 10 % occupancy as the hard operation upper limit for the striplets, this option becomes marginal with a background rate of 20 MHz/cm^2 (safety not included). Striplets modules, read out by the FSSR2 [5] front-end chip, have been already characterized on beam [6], although this chip cannot be the final one because it cannot handle the high rates expected in the Layer0. The most critical aspect of the striplet option is the fast read-out chip required. Once the chip is provided, producing the final Layer0 modules would require only moderate R&D effort. Due to the high number of strips, the design of the module has been rather complex, with the need to accommodate two layers of fanout per side. Furthermore, the hybrid circuit, hosting the f.e. chips, must be placed on the cold flanges in a very tight region, crowded by beam pipe cooling and connections (see Fig. 2).

4. Pixel sensors for the Layer0

The ambitious goal of designing a thin and fast pixel device matching all the Layer0 stringent requirements is being pursued with specific R&D programs: CMOS MAPS, pixel sensors realized on multiple layers with vertical integration technology and hybrid pixels. The latest results on the various pixel options will be presented, explaining the path we are following in exploring the different technologies for the SuperB Layer0.

4.1 Monolithic Active Pixel Sensors

When the material budget is critical, as in the SuperB Layer0, CMOS MAPS are very appealing because in this technology the sensor and readout electronics share the same substrate that can be thinned down to several tens of microns. As the readout speed is the another crucial ingredient,

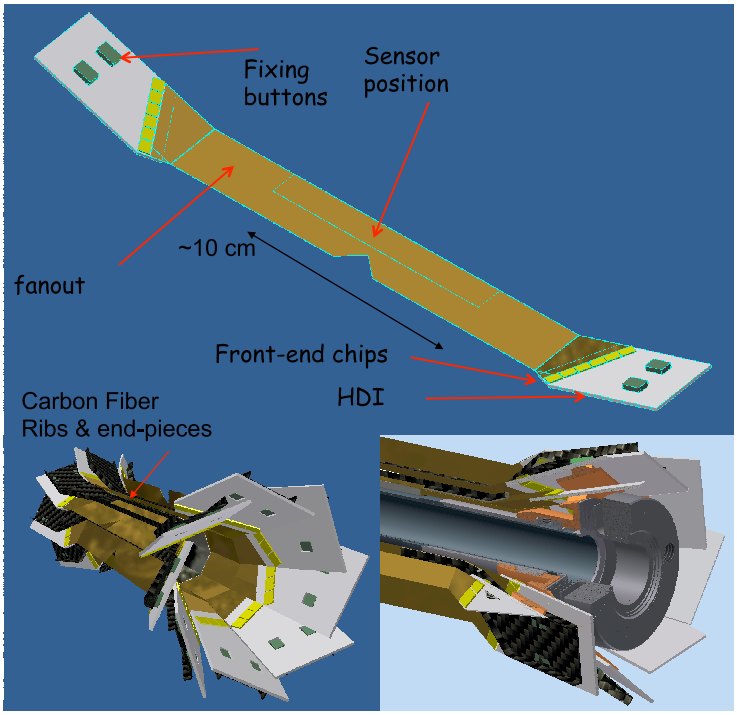

Figure 2: Drawings of the octagonal Layer0 made of striplets modules. In the inset, the striplet modules positioned on the cold flanges with the Be beam-pipe.

we have developed in the last few years a new Deep NWell (DNW) MAPS design [7] that allowed for the first time the implementation a CMOS pixel matrix with in-pixel data sparsification and timestamping [8].

Several prototype chips (the "APSEL" series) have been build using the ST-Microelectronics 130 nm triple well technology and they demonstrated that the proposed approach is very promising for a thin and fast pixel detector. Signal to noise ratio up to 20 have been measured for MIP particles, with a typical cluster signal of about 1000 e^- [7]. The last prototype realized, the APSEL4D chip, a 4k pixel matrix with 50×50 m^2 pitch and a data push sparsified readout with timestamping, has been tested with beam [6] reporting a hit efficiency of 92%, related to the pixel cell fill factor (ratio of the DNW area to the total area of N-wells) which is about 90% in the APSEL design.

Radiation hardness of the DNW MAPS is a critical issue for application in Layer0. A campaign of irradiation with γ-rays from ^{60}Co, up to about 10 Mrad, and with neutrons up to a fluence of about $7 \cdot 10^{12}$ n/cm^2, has been carried out on DNW MAPS devices. Test in laboratory indicated a significant degradation of the charge collection after the final step of neutron irradiation, which corresponds to about one year of the expected equivalent neutron fluence in the Layer0.

A higher level of radiation hardness seems adequate for application in Layer0 and it is shown by CMOS MAPS realized in process with a high-resistivity epitaxial layer [9]. This option is currently under investigation: in July 2011 a new chip of the APSEL MAPS devices has been submitted in the INMAPS 180 nm process[10]. The quadruple well used by this technology can be exploited to

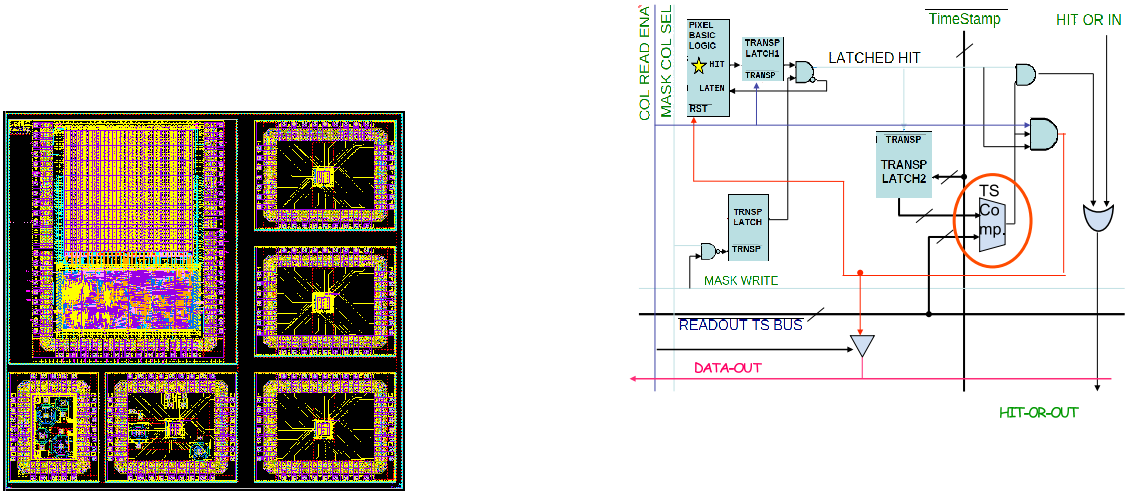

Figure 3: Left: the layout of the chip submitted in the INMAPS, with the 32x32 pixel matrix and the other test-structures. Right: schematic of the in-pixel logic needed for a time-ordered readout.

improve the charge collection. A deep p implant (the fourth well) is able to screen the competitive n-wells of the pmos transistors, preventing them from stealing charge. There also is no need to use large collecting electrodes, small n-well collecting diodes are efficiently working, presenting a lower input capacitance to the preamplifier and thus achieving a better noise vs power trade off. The 25 mm^2 chip (see Fig. 3-left) includes a matrix consisting of 32x32 (50 m pitch) pixels, some test structures and several small 3x3 pixel matrices with the analog signals available to optimize the pixel layouts. The larger matrix implements a new read-out architecture, easily scalable to matrices of 50 Mpixel, developed to sustain the target hit rate of 100 MHz/cm^2. The readout architecture relies on a complex and original in-pixel logic, which provides the timestamp and a time-ordered pixel readout, allowing the chip to be operated either in triggered or data push mode.

The Fig. 3-right schematically describes the adopted read-out. The timestamp (TS) is broad-casted to the pixels. When a pixel is fired (signal above threshold) it latches the current TS. A readout TS enters each pixel and a HIT-OR-OUT signal is generated for columns with all the hits associated to that TS. The sweep on the columns reads only the ones with a positive HIT-OR-OUT. A DATA-OUT word (with one bit per pixel in the column) is generated for the pixels in the active column where there are hits associated to that TS.

VHDL simulations of this architecture have been performed with an input rate of 100 MHz/cm^2 on the full size (1.3 cm^2) matrix. For the triggered mode (operating with a 50 MHz readout clock and 6 s trigger latency) the efficiency reaches 98.2 %, since in this configuration, where the pixel cell act as a single memory during the trigger latency, the associated pixel dead time dominates the inefficiency. For data-push mode the efficiency is greater than 99.9 % but a very high bandwidth is required on the bus. This readout architecture with dense in-pixel logic is extremely interesting because it can be implemented also in vertical integration (see below) without reducing the pixel collection efficiency and improving the readout performance.

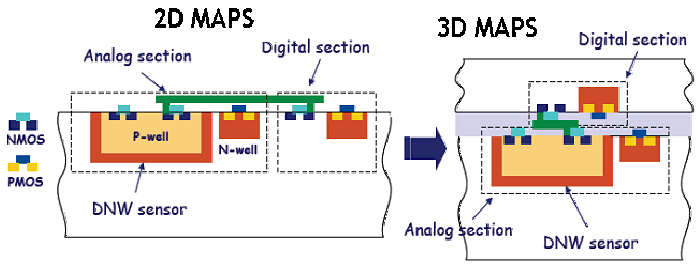

Figure 4: Schematic concept of 2D MAPS, with DNW sensor on a single CMOS tier, and 3D MAPS realized with two CMOS tiers interconnected.

4.2 Vertical Integration Technology

The vertical integration (or 3D) technology promises to allow a series of improvements for DNW MAPS. In these 3D MAPS devices two CMOS layers can be thinned and interconnected by Through Silicon Vias: one CMOS tier can host the sensor with the analog front-end while the other tier is dedicated to the in-pixel digital front-end and the peripheral readout logic (Fig. 4). With this separation of functionalities in different layers, the cross-talk between analog and digital blocks is suppressed and several improvements can be realized: in the collection efficiency, the Nwell competitive area in the sensor is significantly reduced, and to improve the readout performance a more complex in-pixel logic can be developed.

The first prototypes of 3D MAPS, realized by face to face bonding of two 130 nm CMOS wafer in the Chartered/Tezzaron process have been delivered. They include a 3D version of a 8x32 DNW MAPS matrix, with the same sparsified readout implemented in the APSEl4D chip, and two 3x3 matrices with analog readout. In the 3D pixel cell the fill factor has been increased up to 94% and the sensor layout has been optimized; according to device simulation collection efficiency above 98% is expected.

While the wafer bonding of the 3D structures is being completed, the CMOS layer hosting the sensor and the analog front-end is already available and a the characterization of the Chartered process has been performed. The gain calibration was done with the 5.9 keV line of a Fe^{55} source on each pixel of the 3x3 analog matrix. The average pixel gain measured was 304 mV/fC. Using this gain the resulting average pixel noise measured was 44 e- (ENC). The response to MIP particles was evaluated with electrons from a β source. The cluster signal of the 3x3 matrix, shown in Fig. 5, has been fitted with a Landau distribution. The most probable value obtained (41 mV) corresponds to an average cluster signal of 840 e- and a signal to noise ratio for a MIP of 19. These results are encouraging, showing the selected CMOS process is adequate for MIP detection.

We are currently designing a larger MAPS matrix with the cell optimized for the vertical integration process (APSELVI, 128x100 pixels with 50×50 m^2 pitch) and also a second prototype of a front-end chip for hybrid pixel (Superpix1, 32x128 pixels with 50×50 m^2 pitch). Having more room for the in-pixel logic, these two chip will implement the readout architecture already designed for

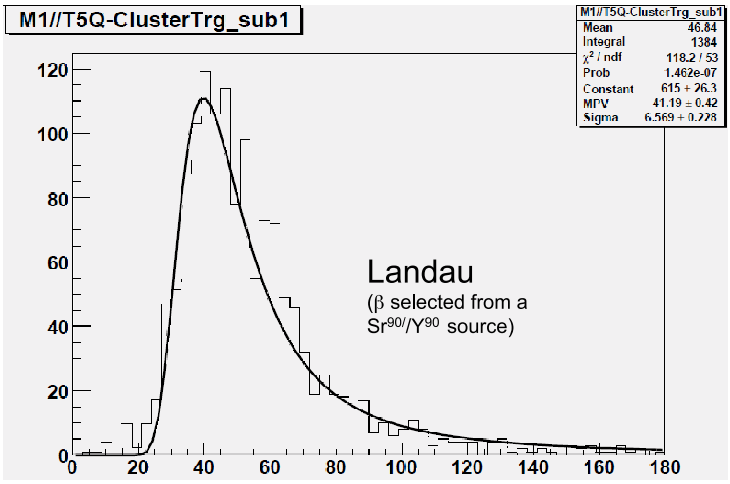

Figure 5: Cluster signal of the 3x3 MAPS matrix with a ^{90}Sr β source.

the INMAPS prototype.

4.3 Hybrid pixels

Hybrid pixels represent a mature option for Layer0, although the material tends to be much higher than for the MAPS option. An R&D program on this option is ongoing in order to meet the required reduction on pixel pitch and in the total material budget with respect to the solution adopted successfully for the LHC experiments. A high resistivity sensor has been fabricated by FBK-IRST: it is 200 m-thick, with n-on-n p-spray isolated pixels. We have realized a first prototype of a front-end chip (called Superpix0, 4k pixels) with 50×50 m^2 pitch, in the ST-Microelectronics CMOS 130 nm process. The data push readout architecture implemented has been derived from the MAPS APSEL4D architecture. The parallelized readout allows a time-sorted hit extraction and a compression of the data output. A VHDL simulation of the readout of a full size matrix (1.3 cm^2) with a background rate 100 MHz/cm^2 gives hit efficiency above 98% operating the matrix with a 60 MHz readout clock. The chip has been successfully tested [11] before and after the interconnection by bump-bonding (realized by Fraunhofer IZM Berlin) with the high resistivity pixel sensor. An ENC of about 80 e- was measured, with the sensor connected, and a very good quality of the interconnections was observed. The hybrid pixel system has been tested with beam in September 2011 and the data are currently being analyzed.

5. Conclusions

The Silicon Vertex Tracker for the SuperB detector is based on the 5-layer BaBar SVT with an additional innermost Layer0 very close to the beam-pipe. The design of this extra layer is a really challenging task for several aspects: high granularity and a fast readout due to the high level of background, radiation hardness, and low material budget to limit the multiple scattering.

Several technologies are currently under study: striplets are foreseen as the starting detector, then at the design luminosity a pixelated solution must be adopted. The extensive R&D activities on hybrid pixel and CMOS MAPS must converge for production soon after the Technical Design Report of the project, expected by spring 2012.

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