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A hybrid module architecture for a prompt momentum discriminating tracker at SLHC

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Abstract

The capability of performing quick recognition of particles with high transverse momentum (more than a few GeV/c) in the inner tracker is deemed essential to keep the CMS trigger rate at an acceptable level at a higher luminosity LHC ($L > 10^{34}$ cm^{-2} s^{-1}). The paper discusses an architecture for a novel tracking module based on a combination of a pixelated sensor with a short strip sensor that would offer such capability.

The critical aspect of the design such as the projected power consumption, the resulting material budget, and the data flow model are discussed and estimates are given. It is also shown that a manufacturable module of this type is well within the capabilities of currently available microelectronic and packaging-assembly technologies.

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1. Introduction

The community of physicists and engineers building detectors for high energy physics experiments has been studying for many years the possibility of designing detectors capable of providing prompt information at a higher level of abstraction than the usual yes/no or simple signal amplitude that most read-out systems today are capable of generating [1]. In the early days of LHC, the generally accepted terminology for such capability was called "feature extraction". Making available at an early stage information such as real geometrical coordinates, direction vectors or deposited particle energy would allow building more sophisticated and fast triggering (filtering) hardware and of course potentially reduce the huge amount of often redundant and rather primitive information that the detectors produce and scientists are obliged to store and analyze.

As the LHC advances toward a higher luminosity and energy phase in the second part of this decade, the CMS experiment is confronted with the difficult problem of improving the fast level 1 filter as to constrain the data rate to remain below 100 kHz [2]. One approach that has been proposed requires the inner tracker to identify particles with high transverse momentum - higher than a few GeV/c - and to make this information quickly available to the Level 1 trigger hardware. One approach when looking for high transverse momentum particles is clearly to use local information inside the tracker to give hints for pairs of hits pointing back to the interaction region that could belong to such particles.

Several architectures have been proposed to build detectors with these capabilities, and this paper illustrates one proposal based on the usage of an all-silicon hybrid short-strip and pixelated module.

2. Requirements

The basic building block for discriminating high transverse momenta particles is a module built out of two detectors at a distance between 1 and 2 mm (see again details in [2]) where one looks for coincidences of nearby hits pointing radially with a sufficiently high transverse direction and forming a so called "stub". To add some vertex pointing capability, a segmentation of between 1 to 2 mm in the Z-coordinate is also required. Stubs detected on different layers must be combined externally to so called "tracklets", to eventually form entire tracks.

The overall tracker system design remains a difficult optimization problem oscillating between the desire to make the overall detector as light as possible, and the hard reality that adding resolution, precision and other features to the detector is done at the expense of power that in some complicated way translates to addition of interfering material (thicker cables for powering, sturdier mechanical infrastructure, larger pipes and heat exchanger contacts for cooling etc.).

Detailed geometrical optimization studies have been done in CMS demonstrating that a sufficiently light arrangement could be achieved by using three double layers of p_T-discriminating modules located at about 10 cm spacing with the first layer at about 25 cm

radius. A more detailed description of a possible overall layout for the tracker can also be found in [3].

3. Proposed module architecture

In CMS several architectures have been studied and two in particular have been explored by this author and others prior to the proposal of the architecture that will be introduced below. First, on a proposal by [4], a module consisting simply of two adjacent short-strip layers has been studied. The so called "Horisberger's" module is similar to a stereo module, but with strips placed in parallel; by performing a simple coincidence between adjacent strips, tracks with high momentum could be easily identified. This module is ideal in terms of simplicity and could be built with the lowest power per unit area; on the other side it has no Z-discriminating capability. A second architecture based instead on two layers of large pixels of about 1.5 x 0.1 mm size has been proposed in [5] and is depicted in Figure 1. This last module would be capable of high quality p_T and Z discrimination, but obviously it suffers from higher power consumption and therefore would lead to an overall higher material budget. In addition, such a module presents significant engineering assembly challenges both from the mechanics and from an interconnect density point of view.

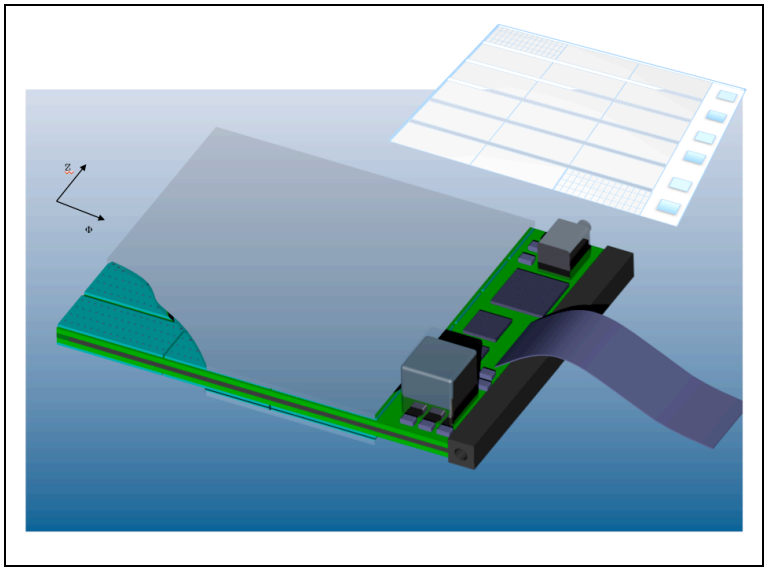

Figure 1 pT discriminating module based on double pixelated layers. The stack consists of two identical layers of sensor and pixel read-out ASIC mounted back-to-back on an interposer. The sensor to read-out ASIC connection is realized with bump bonding techniques similar to those currently used in pixel detectors. All the auxiliary electronics (powering and links) is located on one side of the module. The ASIC to interposer interconnection is realized with a special low-profile wire-bonding technology.

Examination of these two architectures has led us to propose the module depicted in Figure 2. Here one detecting layer is made of a silicon short-strip detector, while the second detecting layer is made of a pixelated detector. A more detailed cross section is shown in Figure 3. The short-strip layer is read-out sideways as a classical strip detector, while the pixelated layer is read-out with ASICs sandwiched together with the sensor, as normally done in hybrid

(i.e. non-monolithic) pixels. In this paper is assumed that both short-strips and pixels will have a 100 μm pitch in ϕ, but a reduction of the pitch to 90 μm is also being considered. The length of these elements in the Z direction is instead determined by considerations on occupancies. Based on estimations of occupancies from Monte-Carlo, it is assumed that these elements will be about 25 mm in length. These dimensions result in a module that could span 50 mm in the Z direction, and if using 1024 channels of 100 μm width, a total of about 10.2 cm in ϕ.

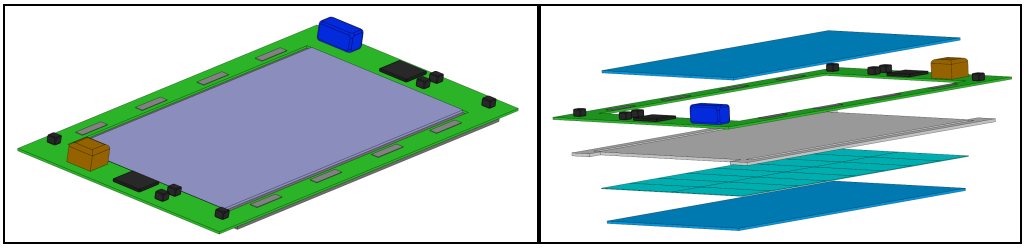

Figure 2 Normal and exploded view of the proposed module. The stack consists of (bottom to top) a pixel detector, a layer of pixel read-out chips, a cooling interposer and spacer, a frame shaped hybrid housing the strip read-out chips and the auxiliary chips and a short-strip detector. The frame hybrid is a high density interconnects Multi-Chip-Module housing the 128/256 channels read-out chips for the short strips. The components on the side represent schematically the auxiliary components such as the DC-DC converters and the opto-links.

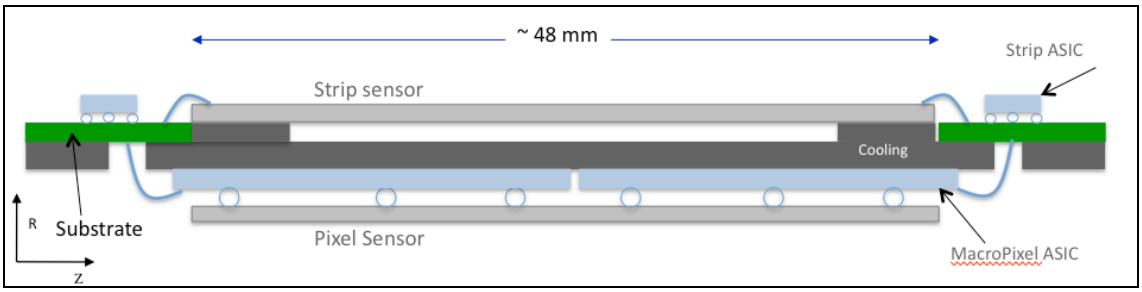

Figure 3 Detail (not to scale) of the module cross section. Notice that this assembly allows wire bonding of the short-strips to the read-out ASICs located on the peripheral frame (MCM), while the pixels are connected to the pixel read-out chips through a relatively low density (200 μm pitch) bump-bonding technique.

The sensing elements in the pixelated layer are logically OR-ed for triggering purposes in the Z direction and therefore act as a single strip and are used to seek for a coincidence in the rϕ plane to determine the appropriate momentum cut. Figure 4 shows the simple logic that would be necessary to look for such a coincidence between the pixel and the strip layers for a window of ± 1 strips around a hit pixel. The width of the acceptance window will clearly be programmable in the pixel chip. The hit information along the Z coordinate is retained in the pixel internal storage and also promptly read out to be combined with the same information in other double layers to search more precisely for particles originating from the vertex region.

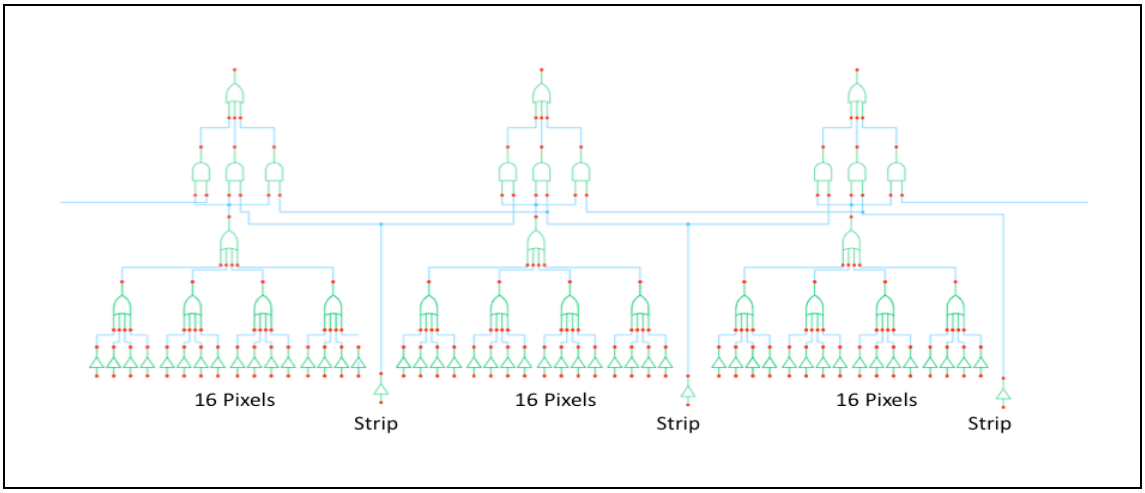

Figure 4 Simplified trigger logic. A coincidence (stub) is produced if a hit is present on a short strip and in the pixel row on top, or immediately left or right of it.

3.1 Read out architecture and integration in a trigger system

As the presence of a high p_T pair of hits has to be made available to the triggering system with the shortest latency, it is important that the read-out path from such a module is optimized for this purpose. A block diagram of the module read-out is shown in Figure 5. Assuming that each module could be equipped with a 3.2 Gbit/sec link toward the counting room and that the link is to be shared between the trigger and the L1 data read-out, the L1 data will be sparsified in the module in order to reduce the bandwidth required to send these data. An estimation based on expected occupancy leads to an L1 data rate lower than 100 Mbit/sec, which will safely almost be ignored in the overall 3.2 Gbit/sec link budget. The trigger info is instead critical and a small toy Monte Carlo has been written to estimate the latency that could be resulting from different occupancies and event types in the detector. The data traffic generated on links by sources such as those shown in Figure 6 has been assumed. For an acceptable event loss probability of 10^{-6}, we computed a modest buffer depth of 7 trigger events in the pixel ASIC and therefore a latency of 7 LHC clock cycles. An asynchronous read-out of the trigger information, clearly requires also that the receiving end re-aligns events in time, and therefore that a small 7 element buffer is available before entering the trigger box.

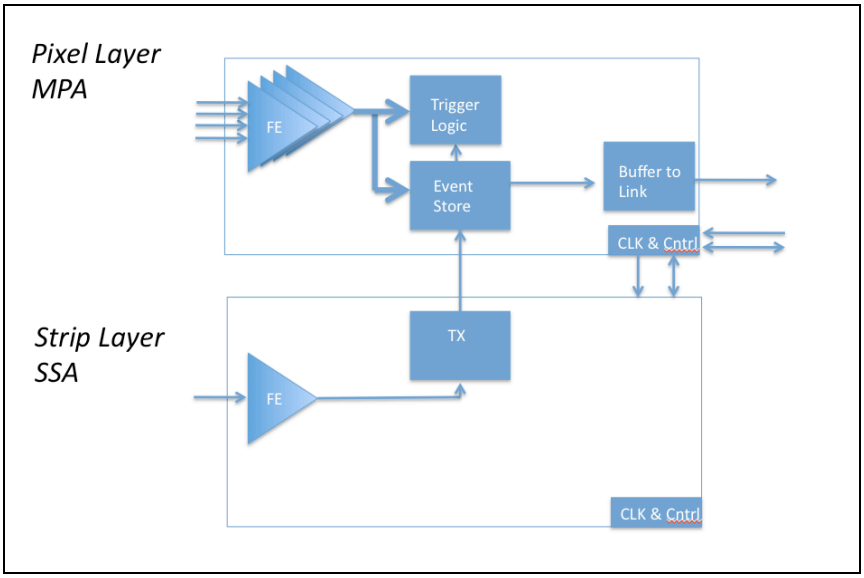

Figure 5 Module read-out data path. The Short-Strip-ASIC (SSA) consists of a front-end circuit and a discriminator, but no event buffering or pipelining. The 128 (or 256) bit hit map in the short strip is transferred to the pixel chip at each bunch crossing. All trigger logic, buffering and data formatting is located in the Macro-Pixel-ASIC (MPA).

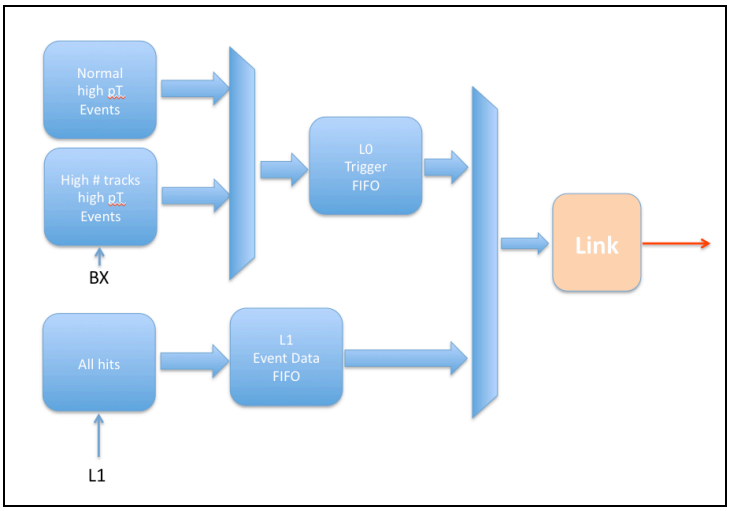

Figure 6 Simplified model of the data read-out flow. Two types of trigger events data sources are assumed ("normal" and "high multiplicity") and traffic from normal L1 data are combined into the link to the counting room.

3.2 Module components

The components constituting the proposed module are described in the following paragraphs separately.

3.2.1 Short-strip ASIC

Assuming a strip length of 25 mm and a pitch of 100 μm a detector capacitance of around 2 pF is expected. It is assumed that the ASIC for the read-out of these strips will be designed for 128 or possibly 256 channels. Similar read-out ASICs are currently being designed also for other trackers, such as the new Atlas tracker at LHC, and are considered as optimized versions of existing chips (APV and CBC in CMS, ABC130 in Atlas, VFAT in Totem etc.). The architecture of such a chip requires a binary output to be made readily available to the Pixel ASIC where actually the coincidence for the momentum cut is performed. Based on experience with present short-strip read-out ASICs and on improvements likely to be achieved by more sophisticated circuit design techniques and more advanced CMOS technologies, a power dissipation of 250 μW/channel has been surmised for this ASIC. Unlike other short-strip ASICs, it is expected that this ASIC will need no L1 trigger pipeline buffering, as the digitized channel information is immediately transmitted to the corresponding pixel ASIC on the same module. This could make the short-strip ASIC potentially very small in the Z dimension (less than 2 mm) and therefore allow a very compact supporting substrate (hybrid) on the side of the module.

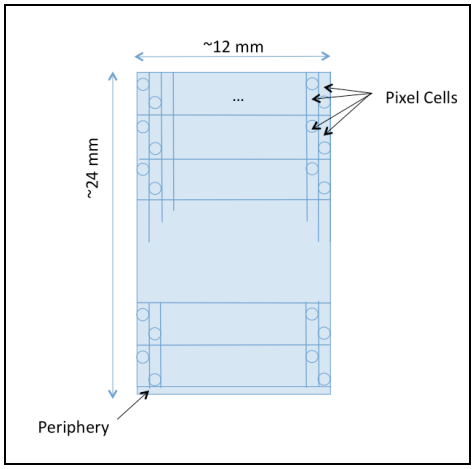

Figure 7 Simplified floorplan of macro pixel ASIC

3.2.2 Macro Pixel ASIC

This is the core chip for the proposed system. It consists of a matrix of 16 x 128 pixels (along Z and ϕ) of dimension 1500 x 100 μm^2, the periphery of the chip is located on just one edge and is expected to house all the circuitry necessary for connecting to the outside world. Given the relatively large area of each pixel density is not a major issue in this design, and a simplified floorplan showing the staggered arrangement of the pad contacts to the sensor is presented in Figure 7. It is expected that such a chip will be designed in a rad-tolerant 130 nm or even 65 nm CMOS technology, the choice being driven most likely by the capability of the technology to offer the largest area chip (this depends on the so called "reticle size" as offered by different ASIC foundries). The Macro Pixel ASIC (MPA) size determines actually the maximum size of a manufacturable module, and therefore a large ASIC of 24 x 12 mm^2 is being

assumed.

The signal path of the front-end of the MPA is rather classical, and consists of the normal preamp-shaper-discriminator front-end followed by a memory buffer storing the pixel hits for later L1 trigger read-out. Once the hit has been discriminated, a block diagram of the remaining digital functionality for triggering is shown in Figure 8. A simple logic is provided performing the OR-ing operation of the channels along the Z direction and the successive AND-ing in an appropriately programmed ϕ window with the incoming hit from the strip ASIC. Cluster reduction, module alignment and coincidence search are all performed in this block.

It should be noted that the trigger logic in this module architecture is implemented in the pixel ASIC and not in the strip ASIC. There are two reasons for this architectural choice: first, the amount of data to be moved is smaller from the strip to the pixel rather than the opposite. Second, the area of the pixel ASIC is constrained by the size of the pixel detector size and is large anyway (in microelectronics terms), therefore allowing the designer to embed easily the trigger logic in the pixel instead of increasing the area of the strip ASIC, which is constrained by the requirement of making the substrate housing these chips as small as possible.

Based on an estimation deriving from a detailed circuit study for the CERN NA62 Giga-Tracker, where a comparable pixel area is used, a dissipation of 80 μW per pixel channel is assumed [6]. Still with this rather aggressive estimate, a ratio of power per unit area of about 4 is expected between the pixel and the short-strip detector.

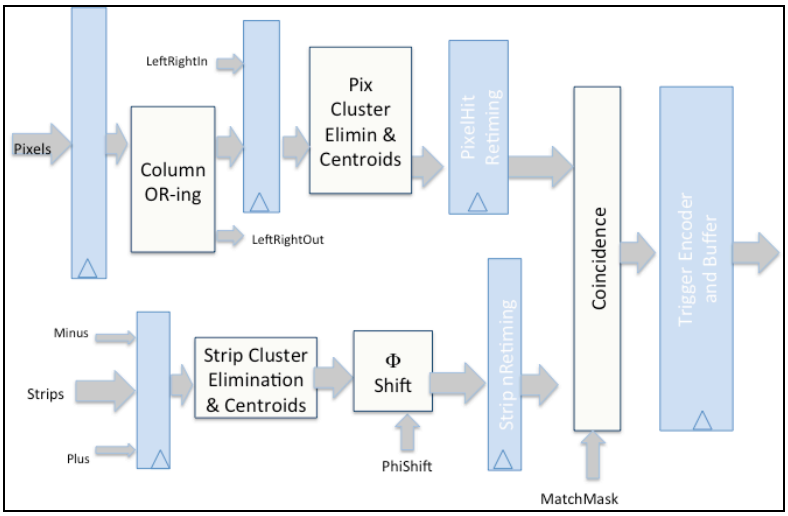

Figure 8 MPA Data Path for Triggering

3.2.3 Link ASIC

A data link ASIC will be necessary to send the trigger and L1 data information to the counting room, to receive the system clock and the local fast and slow control information. This link is a very critical part of the module. Present microelectronic technology available in the HEP community indicates that the power requirement to build a 4.8 Gbit/sec raw capacity rad-tolerant bidirectional link requires around 2 W or 40 pJ/bit [7]. This power consumption has to be reduced drastically to make affordable using one link on each new triggering module. Preliminary studies on the circuit optimization of this link ASIC (providing 3.2 Gbit/s user

capacity, i.e. 80 bits per LHC bunch crossing) through the implementation of serializer, laser driver and transimpedance receiver on an advanced technology (65 nm CMOS) indicate that a power consumption of 0.5 W could be expected. Another critical element for the construction of such a module is the further miniaturization of the opto components (laser diode and receiving photo-diode and the associated driver and receiver chips) that will have to use new customized packaging and interconnect solutions.

3.2.4 Powering

The CMS collaboration has accepted some years ago the challenge of using embedded DC-to-DC converters to reduce the mass of cables bringing power to the tracker. The powering cables and copper on PCBs constitute an important and very visible part of the material profile of the current tracker and their reduction constitutes an absolute must for a future higher performance detector. A preliminary study of the power consumption of the chips discussed above leads to an estimate of about 4.5 W for the whole module. Assuming a 1.2 V supply, an on-module DC-to-DC converter would therefore have to supply some 3.75 A. Unfortunately the opto components above will need also a higher supply voltage of 3 V for operation, therefore some further power converter (step-down or step-up) will be needed. The architecture proposed assumes that these powering elements are installed on each module. Significant advances have recently been made in the miniaturization of these DC-to-DC converters [8], while the size of passive components must also be further optimized to improve miniaturization.

3.2.5 Multi-chip module

A key element of the proposed architecture is the design of an optimized interconnect module used to house the strip ASICs, to connect to the pixel ASICs and to provide support for the auxiliary links and power converters. The first feature of the module is the absence of any interconnect layer (interposer) between the detecting sensors. The sensing stack is composed only of the strip sensor, of some appropriate cooling material such as TPG or equivalent [9] of the pixel ASICs and of the pixel sensor. It is conceivable that while the minimal sensor thicknesses will be dictated by the available sensor technology and acceptable S/N ratio, the ASICs will easily be thinned to 200 μm using standard wafer thinning and chip assembly techniques. In this proposal, the pixel ASICs are actually kept in place by the pixel sensor and do not require a holding interposer. The second feature is the reduction of the size of the frame-shaped module by minimizing the functionality required from the strip ASICs, thus allowing a much reduced frame size around the sensitive area. A study of the material profile of such a frame has resulted in a material estimation of 1.2% of a radiation length (X_0), very close to the estimation for the material of the sensing area.

In order to simplify the manufacturing process and to lower the system cost the interconnect technologies used are rather non-aggressive, on modern standards. For instance, the ASIC wire bonding pitch is limited to single rows at 50 μm while the bump bonding technique required to assemble the pixel ASIC to the sensor is limited to a 200 μm pitch, both well below state of the art industry techniques used even in commodity high volume products [10].

4. Summary

The architecture for a tracking module based on a combination of a short strip layer and a macro-pixel layer has been described with the aim of proposing a tracker capable of extracting promptly the features defining high p_T particles at the high luminosity LHC. An overall power consumption of less than 4.5 W seems to be affordable with new cooling technologies and data rates to be handled are within the reach of a robust link technology which is being finalized.

Significant challenges must still be solved before manufacturing of such a module could start, mainly the reduction of power of the necessary circuitry, the miniaturization of DC-to-DC and opto components, the further simplification and industrialization of the assembly sequence needed to build several thousand such modules.

5. Acknowledgements

The ideas necessary to formulate a possible solution for the construction of complex systems such as the one proposed here are of course only slowly matured through innumerable discussions with friendly, open-minded and critical colleagues. Many people have contributed to this, but in particular I would like to thank the patience of Duccio Abbaneo, Francois Vasey, Walter Snoeys and Marcello Mannelli for helping recognizing weak aspects of this early architecture and for stimulating the search for better solutions.

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