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The ATLAS Insertable B-Layer Pixel Detector

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ATLAS currently develops a new Pixel Detector for the first upgrade of its tracking system: the ATLAS Insertable B-Layer Pixel Detector (IBL). The new layer will be inserted between the innermost layer of the current Pixel Detector and a new beam pipe. The sensors are placed at a radius of 3.4 cm. The expected high radiation levels and high hit occupancy require new developments for front-end chip and sensors which can stand radiation levels beyond 5×10^{15} n_{eq}/cm^2 . ATLAS has developed the new FE-I4 chip and new silicon sensors to be used as pixel modules. Furthermore a new lightweight support and cooling structure was developed, which minimizes the overall radiation length and allows detector cooling with CO_2 at -40 °C coolant temperature. Currently the overall integration and installation procedure is being developed and tested ready for installation in 2013. The paper summarizes the current state of development of IBL modules, first preliminary test results of the new chip with new sensors, the construction of its pixel staves and overall support structure. It will conclude with an outline of the challenges for its installation in the present ATLAS detector system.

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1. Introduction

The present Pixel Detector [1] of the ATLAS experiment [2] at LHC is constructed of three concentric barrels and three discs at either end. The barrels surround the beam pipe at radii of 50.5 mm, 88.5 mm and 122.5 mm respectively. During the runtime of LHC, the ATLAS experiment will collect approximately 300 fb^{-1} of data. The resulting particle fluence, expected at 50 Mrad ionizing dose and 1×10^{15} n$_{eq}$/cm^2 non-ionizing dose in the Pixel Detector, will lead to significant radiation damage of the detector. In particular the innermost layer, the so-called "B-Layer", is expected to gradually loose tracking efficiency due to radiation damage, which will affect the tracking and b-tagging capabilities of the ATLAS experiment.

In order to mitigate the influence of partial loss of efficiency in the present B-layer, the present 3-layer Pixel Detector will be upgraded to a 4-layer pixel detector through the addition of the "Insertable B-Layer" (IBL) [3] detector in the LHC shutdown of 2013. The IBL will be installed, together with a new smaller diameter (47 mm) beam pipe, into the present Pixel Detector, which will be maintained. The IBL sensors and front-end (FE) electronics will be located at a radius of $\approx$34 mm from the beam axis. For a lifetime of 300 fb^{-1} the IBL needs to withstand 250 Mrad of ionizing dose and 5×10^{15} n$_{eq}$/cm^2 of non-ionizing dose with a tracking efficiency of $>$97%. The addition of the IBL will significantly improve ATLAS physics performance in the area of b-tagging and light-jet rejection for the main bulk of data expected at LHC after 2013.

In addition to the improved radiation hardness of the IBL, the front-end electronics also needs to cope with the significantly higher hit rate. With a peak luminosity expected in excess of 2×10^{34} cm^{-2}s^{-1} and a sensor radius of $\approx$34 mm, the present ATLAS pixel front-end chip architecture would cause significant tracking inefficiency due to limitations in on-chip data transfer. This limitation has been addressed in the development of a new front-end chip, the FE-I4 chip [4], which also copes with the increased radiation hardness requirement and has a substantially larger active area (16.8×20 mm^2) than the present Pixel Detector front-end chip. Furthermore the pixel size has been reduced to 50×250 μm^2. The reduced radius of the innermost layer and the smaller pixel length will lead to substantial improvement in impact parameter resolution for the next 4-layer pixel system [3]. To allow further performance gains, the IBL developments are aimed at reducing the radiation length of all inactive parts: most notably with thinning of front-end chips, thin flex circuits and the use of light-weight materials in stave construction. While the radiation length at perpendicular incidence of a present pixel layer is approximately 2.7%, we aim for a total of 1.5% of radiation length for the IBL including all support structures.

2. IBL geometry and layout

The IBL will consist of 14 pixel staves surrounding the beam pipe. Each stave carries 32 FE-I4 pixel chips, which are bump bonded to silicon sensors. The IBL collaboration currently considers two type of sensors: planar n-in-n sensors [1], similar to the present Pixel Detector, and 3D silicon sensors [5]. Both sensor types have been prototyped to IBL module specifications. In case of planar sensors, one sensor carries two FE-I4 chips, in case of 3D sensors, one sensor carries one FE-I4 chip. The staves are inclined by 14 $^\circ$ with respect to the radial direction in order to achieve overlap of active area between staves and to compensate for (a) the Lorentz angle of drifting charges in

the 2T magnetic field in case of planar sensors or (b) the effect of partial column inefficiency with perpendicular tracks in case of 3D sensors. There is no shingling of sensors along z due to the lack of radial space. Modules are glued adjacent on the stave with a physical gap of 200 μm for planar two-chip modules and 100 μm in case of single-chip 3D modules. The 643 mm long active area of a stave corresponds to a pseudo-rapidity coverages of $|\eta| < 3$.

Figure 1 shows a cross-sectional view of the IBL detector, the new beam pipe and the IBL support tube (IST). The 7.3 m long beryllium beam pipe is covered by kapton heating foil and thermal insulation. The staves are mounted around the beam pipe with the modules facing the pipe. The IBL modules are carried by carbon-fibre structures, called "bare staves", which also include 1.5 mm inner diameter titanium cooling pipes. On top of the support stave a multi-layer kapton circuit provides power and readout to each chip. From the end of stave services for power, readout and cooling connect each half-stave to the end of the Pixel Detector, and from there to the power supply, control and readout units in the counting rooms of ATLAS. The data of each chip are read out by VME readout drivers (ROD) without further multiplexing for maximum redundancy. The entire assembly of beam pipe and staves is supported by the 6.6 m long IST inside the present Pixel Detector.

3. Sensors and modules

The silicon sensors chosen for the IBL are planar n-in-n pixel sensors and 3D silicon pixel sensors. Considering the specifications for the IBL the sensor design is driven by several requirements:

- operational with a tracking efficiency of >97% up to a total non-ionizing fluence of 5×10^{15} n_{eq}/cm^2
- maximum operational voltage less than 1000 V
- maximum power dissipation of 200 mW/cm^2 at -15 °C sensor temperature
- minimal inactive edge, typically 200 μm

The planar n-in-n sensor design is largely based on the design of n-in-n sensors used in the ATLAS Pixel Detector [1]. The sensors are manufactured by CiS[1]. The design has been adapted to the IBL needs by reducing the pixel size from 50×400 μm^2 to 50×250 μm^2. The sensors are 200 μm thick. The IBL design features a new design for the guard ring area in order to maximize the possible operation voltage and minimize the inactive edge. The so-called "slim-edge" design, shown in figure 2(a) uses 13 guard rings on the bias side of the sensor to manage the potential drop between bias contact and physical sensor edge. The distance from the last guard to the dicing edge is 100 μm. To maximize the active area, the edge pixels on the electrode side of the sensor are 500 μm long and overlap the guard ring area. Within this overlap the detector operates under-depleted however still sufficient charge is collected so that hits are registered and the area can be considered active. Simulations indicate an inactive edge of 200 μm to 250 μm in this design [6, 7].

[1] CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Erfurt, Germany, http://www.cismst.org/

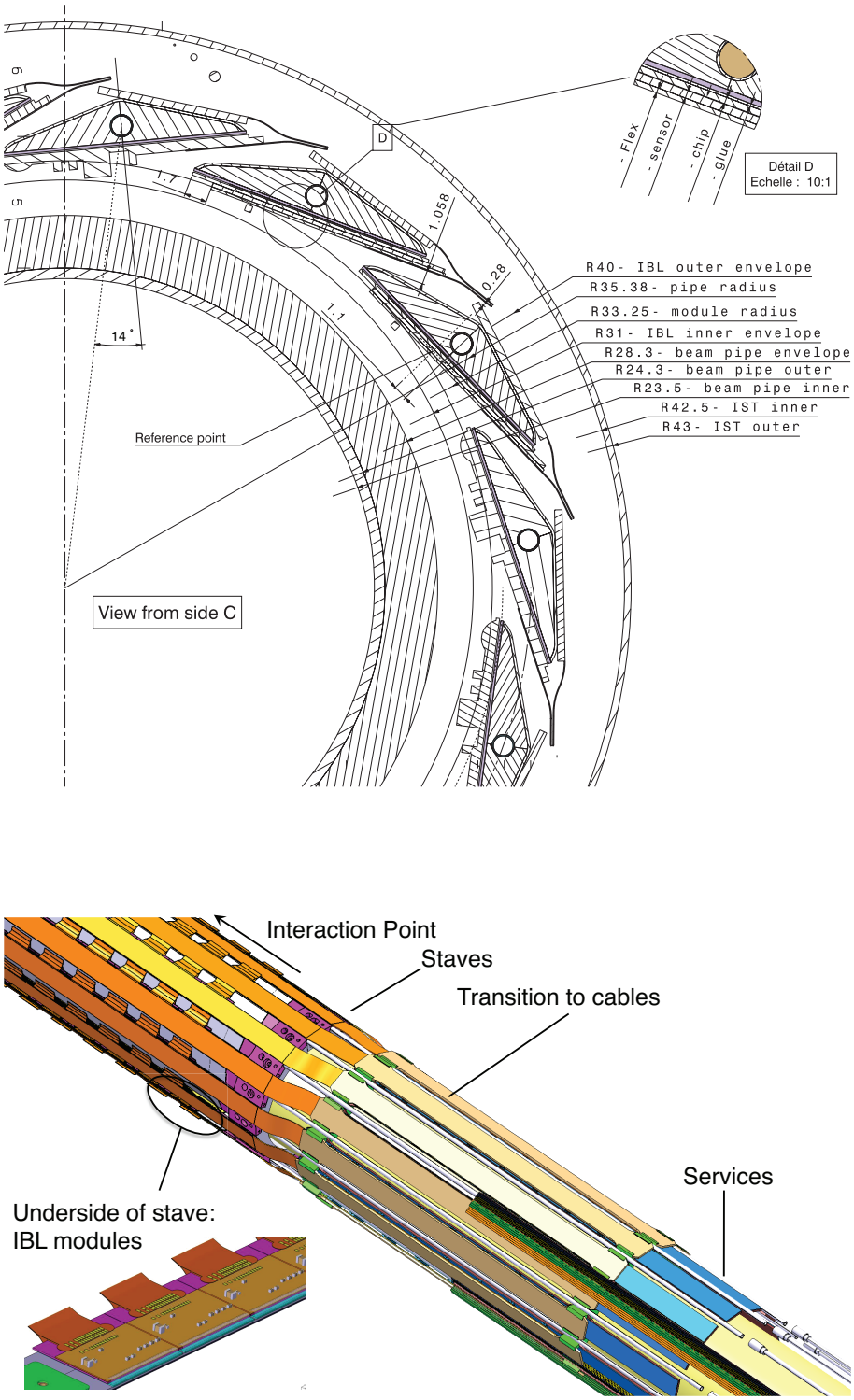

Figure 1: Top: Section view of the IBL, the new beam pipe and the IBL support tube (IST). Radii of envelopes are are given in mm. Bottom: Three-dimensional view of the stave end transition to services and three-dimensional view of IBL modules on stave.

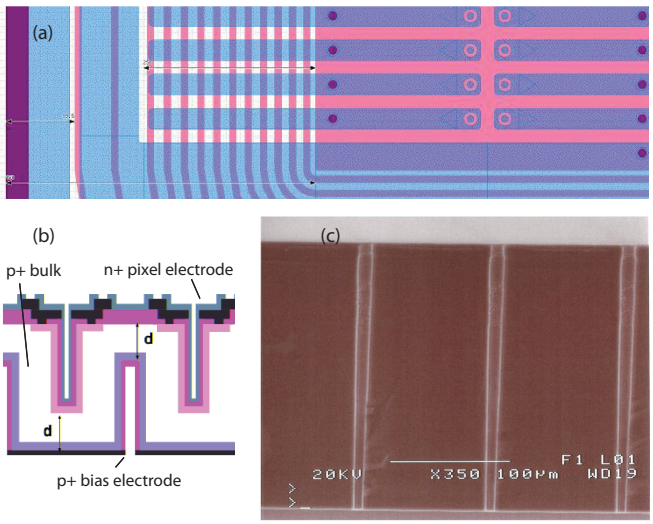

Figure 2: (a) Edge pixel and guard ring layout of the IBL planar n-in-n silicon sensor design. (b) Schematic view of the 3D silicon pixel sensor (c) Micrograph of the deep reactive ion edged (DRIE) columns in a 3D sensor manufactured by FBK.

In the 3D sensor design the measuring and biasing electrodes are edged through the p^+ silicon bulk by deep reactive ion edging (DRIE), as shown in figure 2(b,c). The sensor is depleted between n^+ pixel electrodes and p^+ biasing electrodes. This biasing scheme makes the sensor depletion independent of the sensor thickness. It allows for high field strength and good charge collection after irradiation at moderate bias voltages. The number of n^+ electrodes per pixel can be optimized for given sensor and electronics requirements. For the IBL a design with 2 n^+ electrodes per pixel, surrounded by 6 p^+ biasing electrodes, showed the optimum between maximum collected charge and minimum electronics noise due to detector capacitance [8]. The sensors are 230 μm thick and are manufactured in double-sided processes by CNM[2] and FBK[3]. The sensors manufactured by FBK and CNM share the same top metal layout for identical bump-bonding connection to the FE-I4 front-end chip. Both 3D designs by CNM and FBK feature an inactive guard ring area of 225 μm width. In case of CNM it is formed by a fence of junction columns in the p^+ bulk, which are surrounded by a frame of ohmic columns, in order to sink the edge leakage current. In the FBK design [9] the guard ring area is formed by an array of equipotential ohmic columns, all shorted together, in order to separate the dicing edge from the active area.

The sensor designs for planar and 3D detectors have been extensively prototyped and tested with ATLAS pixel front-end chips. Initial pre-production runs with FE-I4 layout have shown a good sensor yield of approximately 90% for planar sensors and 60% for 3D sensors. The difference in yield is due to the more complex manufacturing steps in 3D detectors. Table 1 summarizes basic sensor characteristics.

The pixel front-end chip FE-I4 is manufactured in the IBM 130nm CMOS process. It features a pixel array of 80×336 pixels. Each pixel incorporates a two-stage amplification/shaper analog

[2]Centro Nacional de Microelectronica, Barcelona, Spain http://www.cnm.es/
[3]Fondazione Bruno Kessler, Trento, Italy, http://www.fbk.eu/

	3D sensor	**Planar sensor**
Active size [mm^2]	16.8×20.0	16.8×40.9
Physical size [mm^2]	18.8×20.5	18.54×41.3
Thickness [mm]	0.23	0.20
Typical depletion voltage [V]	≤ 15	≤ 35
Typical initial operation voltage [V]	25	60
Operation voltage at end of lifetime [V]	180	1000

Table 1: Summary of basic parameters for 3D and planar silicon pixel sensors.

stage followed by a discriminator. A common threshold is applied to all pixels, the pixel DC offset can be adjusted via DACs individually in order to achieve a uniform signal threshold across the chip. For each hit the 4-bit time-over-threshold (ToT) information is stored as measure of the analog charge amplitude. A 2×2 pixel region in a double column share a common digital processing stage, which includes hit buffering, trigger logic and data encoding. The hit buffering at the pixel level resolved the data transfer limitation of the previous design, where any hit was transferred to the end of column for buffering.

The first full chip (FE-I4A) has been submitted in 2010 and has been extensively tested without and with sensors as well as in irradiations and test beams. A lot of 12 wafers has been tested in wafer probe tests, on test cards and in assemblies with sensors. In those tests the digital and analog functionality of the FE-I4 could be well demonstrated and a yield of typically 40 good chips on a wafer of 60 chips was shown. The preliminary noise measurement has shown a typical r.m.s. noise of 80 e^- without sensor, 130 e^- to 140 e^- with un-irradiated sensors and 150 e^- to 160 e^- with irradiated sensors, pending further gain calibration, which is currently ongoing. In testbeams and laboratory tests the FE-I4 could routinely be operated with thresholds of 1600 e^- with both sensor types, which is a factor two lower than the present FE-I3 pixel chip in ATLAS operation.

More than 80 FE-I4-sensor assemblies have been bump-bonded by IZM[4] using SnAg solder bump-bonding to obtain IBL prototype modules for tests of module performance. Due to the large chip size we expect significant bowing of the chip during the reflow of solder bumps. If the out of plane bow exceeds 20 μm, edge pixel can be expected to be disconnected. To avoid this edge disconnection either a thick chip or a handling wafer on top of a thin chip is needed. Measurements at IZM have shown that a chip thickness of ≈450 μm for the FE-I4 chip size would be required to avoid disconnected bumps on the chip edge. This would present a significant amount of material to the overall IBL radiation length budget. To avoid this excess material a handling wafer process has been devised: the chip is thinned to between 100 and 150 μm thickness and a glass handling wafer is bonded to the thinned chip wafer using a photo-sensitive adhesive. After the flip-chip and reflow process the glass is removed by means of laser exposure of the adhesive. The first single- and two-chip thin IBL modules have been successfully assembled using this process.

Most of the prototype FE-I4-sensor assemblies, usually single-chip assemblies, have been mounted on test PCBs for tests in source tests, in testbeams and after irradiations. Figure 3 shows the signal distributions as measured on planar and 3D sensor assemblies with FE-I4 in the lab using

[4]Fraunhofer IZM, Berlin, Germany, http://www.izm.fraunhofer.de/

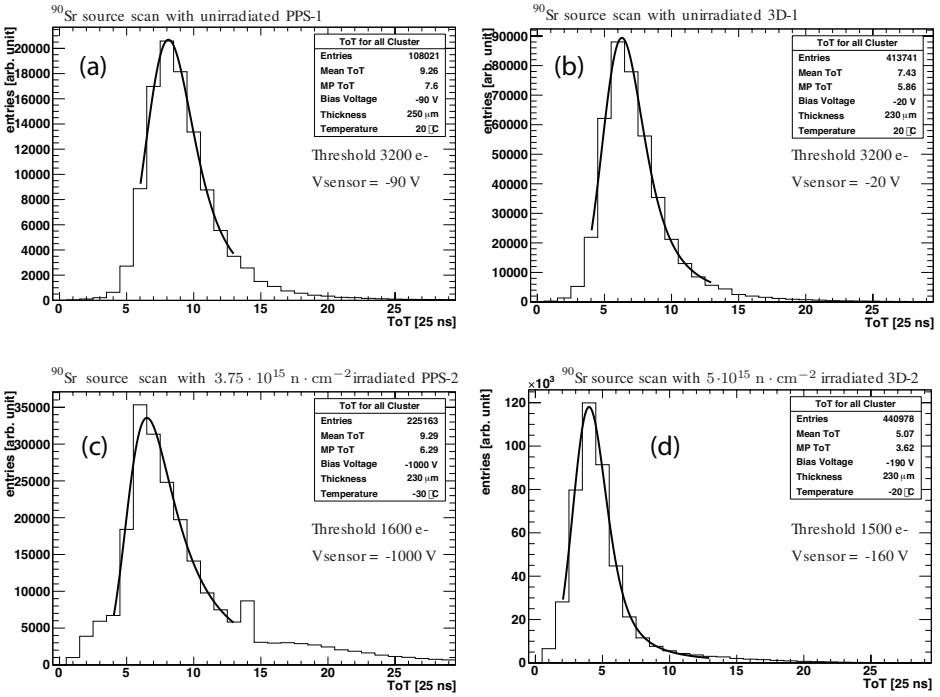

Figure 3: ToT signal distributions measured in a ^{90}Sr source scan on FE-I4 IBL prototype modules with (a) un-irradiated planar pixel sensor, (b) un-irradiated 3D pixel sensor (c) neutron irradiated planar pixel sensor (3.75×10^{15} n/cm^2) and (d) neutron irradiated 3D pixel sensor (5×10^{15} n/cm^2). Planar and 3D assemblies were tested with different ToT calibrations, hence ToT counts cannot be directly compared between planar and 3D assemblies. Un-irradiated and irradiated assemblies of the same detector type use identical calibration.

a ^{90}Sr source to generate hits in the sensor. The collimated source is located above the chip-sensor assembly and the readout is triggered by a scintillator below the assembly, in order to measure only e^- passing through the detector. The top two figures show the Landau ToT distribution as measured on a planar sensor assembly and 3D assembly respectively. The two measurements confirm the full charge collection in planar assembly and 3D assembly. The bottom two figures show the ToT distributions of a planar assembly and 3D assembly, which have been irradiated with neutrons to 3.75×10^{15} n/cm^2 and 5×10^{15} n/cm^2 respectively[5]. The irradiated modules were operated at -20 °C during the tests. On the irradiated assemblies the Landau distribution can be identified well above the threshold. Its amplitude is reduced due to charge trapping in the irradiated sensors. The peak at ToT=14 in figure 3(c) can be considered as an artifact of the 4-bit ToT resolution in the front-end chip. Further assemblies have also been tested after irradiations at the Karlsruhe Institute of Technology (KIT) (Karlsruhe, Germany) with 25 MeV protons.

Several planar and 3D sensor assemblies with FE-I4 were tested at the CERN SPS accelerator with 180 GeV pions to measure their efficiency, charge sharing between pixels and spatial resolution. First preliminary analysis of the testbeam data confirmed a tracking efficiency of >99% on

[5]Irradiations were carried out in the TRIGA reactor of J. Stefan Institute, Ljubljana, Slovenia

un-irradiated planar and 3D IBL prototype modules. Analysis of data taken on irradiated modules is currently in progress.

4. Stave - cooling and support

The function of the IBL carbon-fibre (CF) stave is to support the detector modules around the beam pipe, provide cooling to them and carry the multi-layer flexible circuit which electrically supplies and reads out the front-end chip. In the design of support stave the following key requirements were taken into account: minimal bow as function of temperature (less than 150 μm in operation range of room temperature to -40 °C), minimal radiation length of support (target $X/X_0 \leq 0.5\%$) and high thermal conductivity in order to maintain the sensors cold enough to avoid thermal runaway. The staves are cooled by an evaporative CO_2 cooling system [10]. CO_2 cooling is chosen over the present ATLAS Inner Detector C_3F_8 because it allows for a 10 °C lower coolant temperature for the benefit of lower sensor temperature and enables us to use smaller diameter cooling pipes in the stave, which minimizes material. The 14 staves are routed individually up to a common manifold, which can be accessed for maintenance. The chips are supplied and readout through a flexible circuit, which serves a half stave and includes common power lines of groups of 4 chips, common clock and command lines for groups of two chips and data output lines for each chip. Furthermore it routes HV lines to the sensors and temperature measurements from NTC sensors to off-detector control. We currently develop two technologies for the IBL flex circuit: a multi-layer mixed Al-Cu design, where layers are interconnected through vias, and a Al-only design, where layers are interconnected through tap-bonding. Prototypes of both are under tests. The flex circuit is expected to contribute between $X/X_0 \approx 0.12\%$ to $X/X_0 \approx 0.2\%$, depending on technology choice, to the overall IBL radiation length.

Figure 4 shows photographs and drawing of a completed full length support stave. The carbon-fibre stave is constructed as shell formed by the separately cured "omega" piece and face plate. Omega and face plate are manufactured from 3 plies of K13C/RS3[6] carbon-fibre pre-preg fabric. The face plate and face plate uses a layup of $(0°/90°/0°)$[7] fibre orientation. The choice of a high Young modulus fibre raw material, the shape of the omega and shell structure formed by face plate and omega give the carbon-fibre stave its stiffness. The carbon-fibre shell is filled with pre-machined carbon foam[8]. The carbon foam transmits the module generated heat from face plate to cooling pipe. Carbon foam with a density of 0.22 g/cm^3 and a thermal conductivity of $K \approx 30$ W/mK was chosen as a reasonable compromise of low mass and high thermal conductivity. The cooling pipe is a grade 2 titanium pipe with an inner diameter of 1.5 mm and a wall thickness of 0.1 mm. The face plate provides stiffness to the stave, in particular it helps to avoid stave deformation under thermal expansion and contraction due to the CTE mismatch of carbon-fibre shell and titanium pipe. Furthermore it avoids the absorption of module glue into the foam. Glue absorption into the foam during the module-to-stave loading significantly increased the stave weight in prototype tests. Tests with parylene coating of the foam surface, instead of a face plate to avoid glue

[6] Provided by TenCate, USA http://www.tencate.com/

[7] 0 ° corresponds to the axis of the stave

[8] Provided by Allcomp Inc, USA, http://www.allcomp.net/

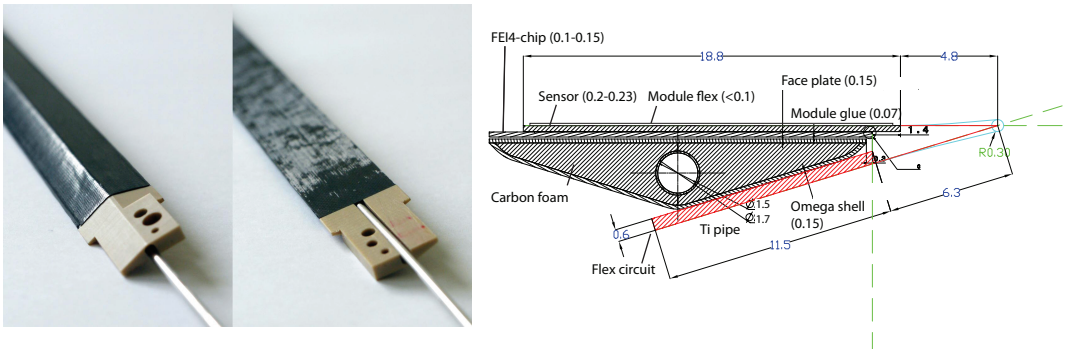

Figure 4: Photographs of a complete full length carbon-fibre stave with cooling pipe (left). Stave cross section drawing with dimensions in mm (right).

absorption, showed that a thickness of $>50\ \mu$m would be required, which deteriorated the thermal figure of merit as measured on prototype staves by nearly a factor 2.

Several tests on prototypes and finite-element analysis of the structure have been used to optimize the structure for the required mechanical and thermal specifications while maintaining a low-mass design. The thermal performance of prototype staves has been measured on several different designs. The thermal performance of the stave is characterized by the thermal figure of merit,

$$\Gamma = \frac{\Delta T}{\delta p} \left[\mathrm{K}\cdot\mathrm{cm}^2/\mathrm{W}\right] \tag{4.1}$$

where ΔT is the temperature difference between the sensor and the inner pipe wall, and δp is the area density of the module power. Multiplying this value with the power density δp $\left[\mathrm{W}/\mathrm{cm}^2\right]$ entering into the stave gives the temperature difference between the inner surface of the pipe and the sensor, hence lower Γ results in lower sensor temperature. We measured on the final design a thermal figure of merit of 13 $\mathrm{Kcm}^2/\mathrm{W}$, well below the requirement limit of 20 $\mathrm{Kcm}^2/\mathrm{W}$. Prototype staves with heaters to simulate chips have been tested on full length cooling lines supplied by a CO_2 cooling plant of IBL specification. Due to pressure drops in actual-length distribution lines, the cooling pipe temperature is elevated by 5 °C over the nominal coolant temperature of -40 °C as shown in figure 5. Figure 5 shows the temperature and pressure profile along the length of the cooling loop. The calculation yields a maximum sensor temperature of -24 °C under maximum power load condition of sensor and chip.

5. Integration and installation

The integration of the IBL proceeds in several steps: (1) gluing of modules to staves, (2) quality assurance tests after loading at loading site and ATLAS surface integration building (SR1), (3) brazing of titanium inlet and outlet cooling pipe extensions to the stave, (4) mounting of staves around the new beam pipe in SR1, (5) connection of power and readout services to stave and routing of services along the beam pipe, (6) final surface test of IBL before installation. The loading of modules is based on manual gluing of modules using precision reference jigs. Tests with prototype

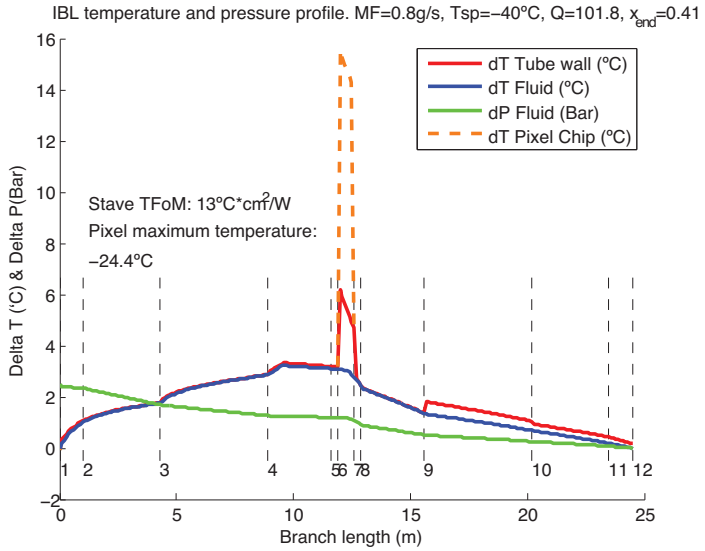

Figure 5: Calculation of cooling line pressure and temperature for a full IBL cooling loop based on measured values of stave thermal conductivity and heat-transfer-coefficient.

modules are currently done to qualify the process with respect to unchanged module performance, thermal performance after mounting and mechanical precision of module positioning. The required precision of $<10\ \mu$m positioning has been demonstrated. After module loading the module position on the stave is surveyed with a 3D coordinate measuring machine with a precision of $\approx 2\ \mu$m. The modules are tested before and after mounting for disconnected bumps and electrical function of modules (digital function, threshold tuning, noise measurement). Once a stave is completed, it is connect to a 100 W CO_2 cooling plant to qualify the stave for warm and cold operation. Inlet and outlet cooling pipes are connected by brazing. Brazing is chosen over welding in order to minimize risks of ESD damage to the chips on stave. Stave pipe, extension pipe and a Ti-sleeve are heated by induction. After a stave is completed for integration it is mounted around the prepared new beam pipe in SR1. Electrical services are connected to both ends and a connectivity test is carried out. Once all staves are mounted we plan to operate the full IBL on the surface for several months to gain operational experience. All of the above procedure is being developed and verified on a 1:1 scale mockup of the full IBL, on which also thermal tests are carried out (e.g. for test of beam pipe bake-out procedure).

In parallel to the final integration of the IBL, its installation is prepared in the cavern in several steps: (1) ATLAS endcaps are moved to a park position in order to gain access to the Pixel Detector which includes the present beam pipe, (2) the beam pipe needs to be removed while the Pixel Detector stays in place. For this operation it is necessary to cut off the beam pipe flange on one side and insert an active tension system into the beam pipe, called “Long Guiding Tube” (LGT). The LGT will actively control the bow of the beam pipe during its extraction through a pre-tensioning system combined with a laser and CCD measurement system, in order to avoid a collision of beam pipe and Pixel Detector during the extraction. The LGT measurement system is based on the Rasnik principle [11]. (3) Using the same LGT a carbon-fibre tube (IST) is inserted into the Pixel Detector.

The IST is constructed of up to 8 layers of carbon-fibre pre-preg. Two full size prototypes have been constructed with different layups and fibre raw material, one uses K13C fibres and one of M55 fibres. Both ISTs are currently under mechanical test. In order to develop, verify and practice this complex and risky operation we constructed a 1:1 scale mockup of the installation region of the ATLAS Inner Detector. Once the IST is inserted in the Pixel Detector and the IBL final surface tests are completed the IBL is transported to the cavern and inserted into the IST. Cable and pipe connections to the end of the IBL packages are done and the detector is commissioned in ATLAS.

6. Summary

ATLAS currently develops and constructs a new pixel detector for the first upgrade of its tracking system: the ATLAS Insertable B-Layer Pixel Detector (IBL). The new layer will be inserted between the innermost layer of the current Pixel Detector and a new beam pipe. A new generation of pixel front-end chip has been developed and tested extensively with planar and 3D silicon pixel sensors for the IBL. The overall support and cooling system was prototyped, based on carbon-fibre staves cooled with a evaporative CO_2 system. Production of sensors, chips, modules and staves has started. The construction and installation is expected to be completed in the LHC shutdown of 2013.

References

[1] G Aad et al, "ATLAS pixel detector electronics and sensors ", 2008 JINST 3 P07007.

[2] The ATLAS collaboration,"The ATLAS Experiment at the CERN Large Hadron Collider ", 2008 JINST 3 S08003.

[3] The ATLAS collaboration, "Insertable B-layer, technical design report", CERN-LHCC-2010-013.

[4] M. Barbero et al., "FE-I4,the new ATLAS pixel chip for upgraded LHC luminosities", Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, October 30ÐNovember 3, Knoxville, U.S.A. (2010), ATL-UPGRADE-SLIDE-2009-319.

[5] S. Parker, C. J. Kenney, J. Segal, "3D: A proposed new architecture for solid-state radiation detectors", Nucl. Instrum. Methods A, vol. 395, no. 3, pp. 328-343, 1997.

[6] M. Benoit, A. Lounis, N. Dinu, "Simulation of guard ring influence on the performance of ATLAS pixel detectors for inner layer replacement", JINST Vol. 4, No. 3, P03 025, March 2009.

[7] M. Benoit, A. Lounis, N. Dinu, "Simulation of Radiation Damage Effects on Planar Pixel Guard Ring Structure for ATLAS Inner Detector Upgrade", IEEE Trans. Nucl. Sci., Vol 56, no. 6, pp. 3236-3243, December 2009.

[8] C. Da Via et al. "3D active edge silicon sensors with different electrode configurations: Radiation hardness and noise performance", Nucl. Instrum. Methods A, vol. 604, pp. 505-511, 2009.

[9] G.-F. Della Betta et al., "Development of modified 3D detectors at FBK", Nuclear Science Symposium Conference Record (NSS/MIC), 2010 IEEE, Nov. 2010, pp. 382-387.

[10] M. van Beuzekom, A. Van Lysebetten, B. Verlaat, "CO2 cooling experience (LHCb)", Proceedings of Science, Vertex 2007, 16th International Workshop On Vertex Detectors, Lake Placid, NY, USA, 23 - 28 Sep 2007, pp. 009, 2007.

[11] P. Duinker et al., Nucl. Instr. Methods A , vol. 273, pp. 814 - 819, 1988.