PROCEEDINGS OF SCIENCE

The UniBoard

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The UniBoard, a Joint Research Activity in the RadioNet FP7[2] programme, has as its aim the creation of a generic high-performance computing platform for radio astronomy, along with the implementation of several different applications (correlator, digital receiver, pulsar binning machine). It is a 3-year project, and kicked off on January 1, 2009. Now past its half-way point, the first prototype board has been delivered and is undergoing tests, and design documents and a large amount of firmware have been produced. The board has generated quite a lot of interest in the radio-astronomical community, because of its high computing and I/O capacity, its potentially excellent computing/power consumption ratio and its use of generic interfaces. At this time concrete plans exist to use it as the basis for the next-generation EVN correlator, the APERTIF correlator and beam former system and at least one all-station LOFAR correlator.

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1. Introduction

The concept underlying the UniBoard was originally proposed by Sergei Pogrebenko, system scientist at JIVE, in the late 90s. As one of the architects of the MarkIV correlator [1], he knew like no other the difficulties and technological pitfalls involved in the construction of such a complex instrument, consisting of many separate custom-made electronic components. A single-board, all-station correlator would do away with the need to transfer large, highly synchronized data streams between all these different components, with their associated complicated messaging systems and timing issues. Such a board should have all the CPU power that could be fitted on, in the form of Field Programmable Gate Arrays (FPGA), and as much I/O capacity as possible. However, in those days FPGA technology was not far enough advanced to make this feasible.

When the preparation for the RadioNet FP7 proposal got underway in 2007, the situation had changed completely, with new generations of FPGAs combining massive computing power with ease of programming and fast development. The concept now became the basis for the UniBoard, one of the Joint Research Activities (JRA) in RadioNet FP7.

2. The project

The aim of UniBoard was to create an FPGA-based, scalable, generic high performance computing platform for radio astronomy, along with a number of demanding applications. Originally the collaboration consisted of 7 participants, and in the course of the project two more partners joined. The original partners and their roles in the project were:

- JIVE: project lead, VLBI correlator
- ASTRON: hardware development
- University of Manchester: pulsar binning machine
- INAF: digital receiver
- Unversity of Bordeaux: digital receiver
- University of Orléans: RFI mitigation in pulsar binning application
- KASI: VLBI correlator

later joined by:

- Shanghai Observatory: VLBI correlator
- University of Oxford: all-station LOFAR correlator

At this time the VLBI correlator, digital receiver and pulsar binning machine are all under development, while the RFI mitigation project has expanded to include both pulsar binning and digital receiver applications. Work is expected to start soon on an APERTIF correlator and beam former (ASTRON), all-station LOFAR correlators (ASTRON + University of Amsterdam, University of Oxford). Several other applications are being considered.

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3. The hardware

During a series of meetings, which started well before the official start date of the project, an inventory was made of the hardware requirements posed by the different applications. Considerations of price, availability and pin lay-out led to the selection of the Altera Stratix IV EP4SGX230KF40C2 chip (40 nm, 1288 18x18 multipliers, 14.3 Mb internal block RAM, 24 + 12 transceivers). With 1288 multipliers at 400 MHz each of these chips could yield a maximum of about 0.5 TMAC/s.

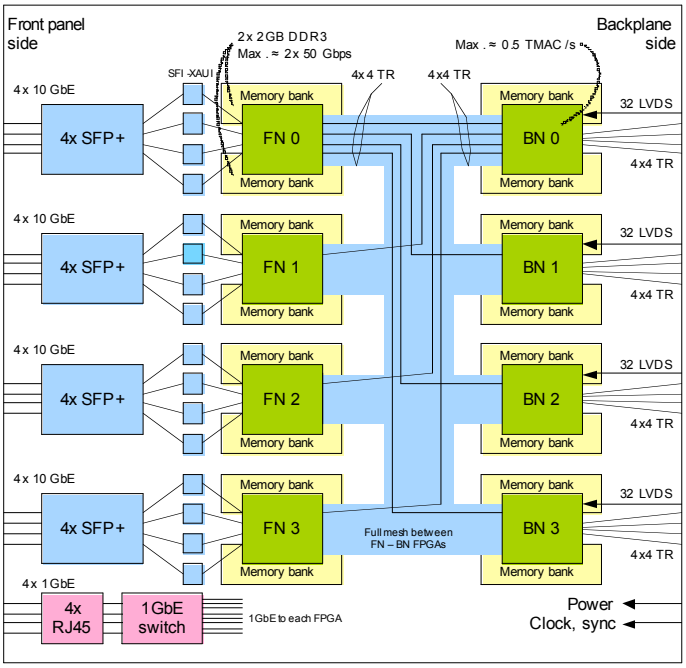

Figure 1: high level UniBoard design

The actual board design was in the hands of Gijs Schoonderbeek and Sjouke Zwier, digital engineers at ASTRON. A configuration of eight FPGAs per board was found to be optimal in terms of computing power, power consumption, density and complexity of the board (Figure 1). Each FPGA is connected to two DDR3 memory banks, mounted on the back side of the board. Four times four 10-GbE links connect to the front nodes (FN) via four SFP+ cages. A high speed mesh connects each FN to all back nodes (BN). The BNs in their turn connect via four times four 8-bits LVDS to a backplane connector. To make the board completely symmetrical, a 10G break-out board (the XGB) has been designed in the form of a mini-backplane, with a total of 16 CX4 connectors (Figure 2).

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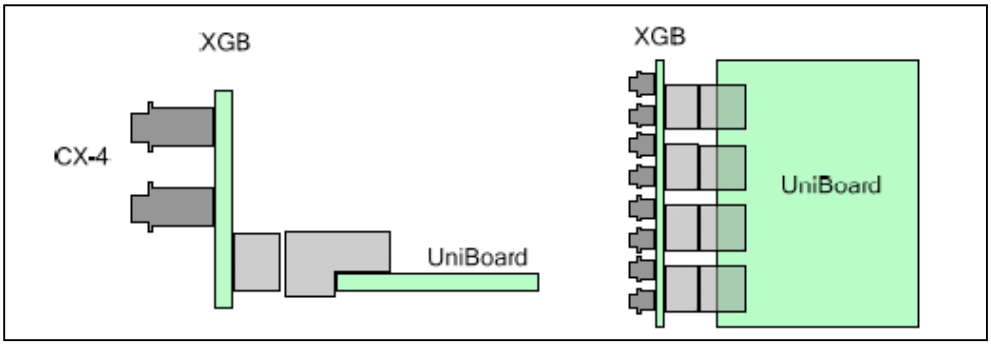

Figure 2: UniBoard with XGB mini backplane

All FPGAs are connected via an onboard 1GbE switch with four RJ45 connectors. The central power supply of -48V is distributed on the board via DC/DC convertors and regulators, the PCB itself is 14 layers. Control and configuration are done via the embedded NIOS processor.

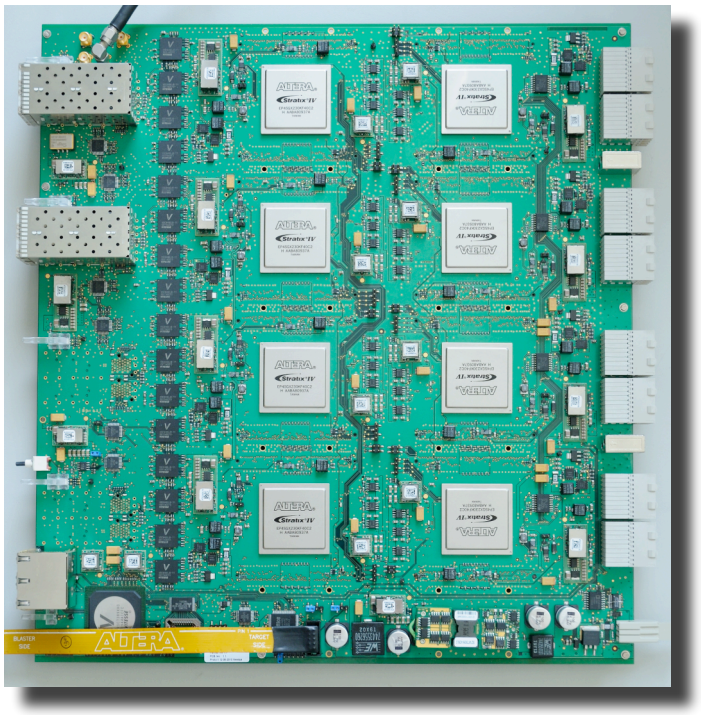

Figure 2: prototype UniBoard, deliverd May 17, 2010

The actual PCB production and board assembly were outsourced. The prototype was delivered May 17, 2010 (Figure 2) and currently the board is undergoing tests. To date, no major design flaws have been identified, although power consumption at full load has turned out somewhat higher than the original estimate (~400W versus 280W). After a review of the modified design, a production run will follow at the end of 2010.

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4. The applications

Throughout the board development phase, work on the various applications progressed; design documents were produced and refined, simulations were done and actual VHDL code was written. All documentation is posted on the project wiki, and all code is shared through a common repository. Of course, the speed of development will pick up considerably once the partners receive the hardware.

The board control is being written in Erlang, a high-level language that provides robustness and completeness and enables a very short code development cycle. At the same time, a general correlator control system is being designed at JIVE.

The most demanding application is without doubt the correlator. Several configurations for different applications are being considered, illustrated in Figures 3 and 4.

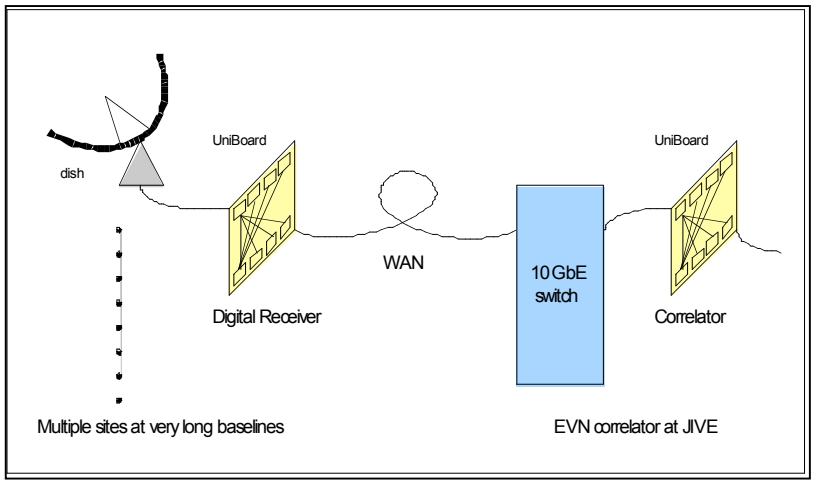

Figure 3: UniBoard as digital receiver and VLBI correlator, connected via internet

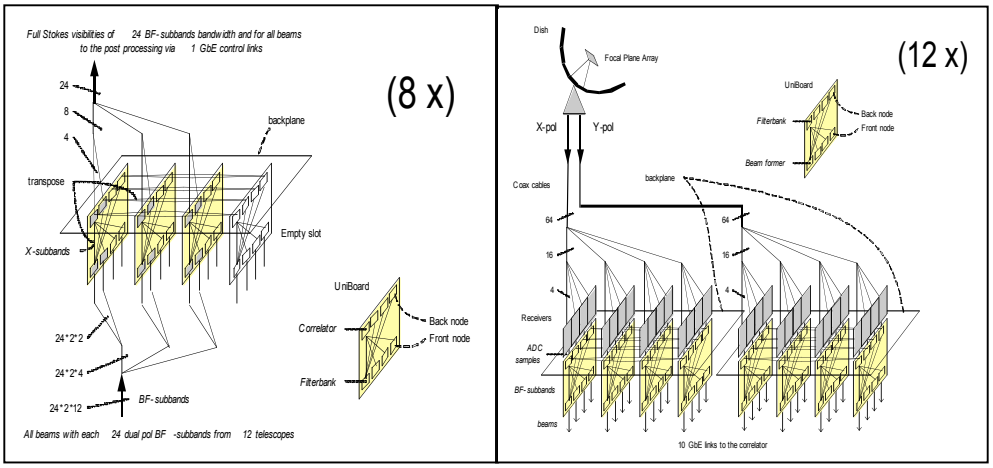

Figure 4: UniBoard as APERTIF correlator (left) and beam former (right), interconnected via a custom-made backplane, with ADCs connected to the opposite side of the backplane

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5. Conclusion

The UniBoard project is well on its way. The performance of the prototype board has met the specifications without revealing any major design flaws. A production run will take place at the end of 2010 and the hardware will be distributed to the partners in early 2011. At the end of 2011 a number of working applications will be in place, that will demonstrate in practice the capabilities of the platform. Finally, this project has helped to position the RadioNet engineering community and demonstrate its excellence in a field that will only grow in importance as the construction of SKA gets underway.

References

[1] A. Whitney et al., *Mark 4 VLBI correlator: Architecture and algorithms*, RADIO SCIENCE, VOL. 39, RS1007, 24 PP., 2004

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