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Serial Power Distribution for the ATLAS Tracker Upgrade

John Matheson[1]
Rutherford Appleton laboratory
Chilton, Didcot OX11 0QX, UK
E-mail: j.matheson@rl.ac.uk
On behalf of the ATLAS Tracker Upgrade Serial Powering Collaboration

At SLHC, the number of detector channels in the ATLAS Semiconductor Tracker must increase by a factor 10, to cope with the increased luminosity. Currently, every detector module has its own power cable, known as independent powering (IP). This arrangement will no longer be tenable, due to cable volume and power losses. A promising alternative is to build supermodules, with many readout hybrids connected in a serially powered chain. This has benefits of simplicity, lower mass and reduced power losses. Such a chain uses constant current, maintaining the supply voltage using variable shunt regulators. The readout hybrids float at different potentials relative to ground and this results in particular technical challenges. Grounding, shielding and data transmission are modified with respect to the conventional arrangement. Serial powering has been demonstrated successfully in the laboratory, using discrete components. Recently, custom components have been produced and test results are very promising. These include the ABCN-25 readout ASICs and the SPI serial powering regulation ASIC, both in 250nm CMOS. The latest measurements from testing of the new custom electronics are presented and future plans are outlined. Proposals are made for the system architecture of a serially powered supermodule for the ATLAS Tracker Upgrade.

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1.Introduction

1.1 The ATLAS Semiconductor tracker (SCT) and the ATLAS Tracker Upgrade (ATU)

In ATLAS, the SCT tracks particles from beam collisions within a magnetic field. Its architecture takes the form of a series of barrels in the central region and discs in the forward regions, instrumented by Si detector modules. Each module [1] is based around back-to-back single-sided silicon microstrip detectors and carries twelve 128-channel readout integrated circuits (ROICs), known as ABCDs. Two chains of power cabling per module connect it to the low voltage (LV) and high voltage (HV) power supplies in the experimental cavern. The SCT comprises a total of 3.2 million channels.

The luminosity of the LHC machine will be upgraded over the coming years and so the occupancy of the detector will increase. An upgraded Tracker, with 34 million channels, will be needed. It is proposed that the upgraded Tracker will include a central region instrumented by detector staves arranged into barrels. This paper will focus on barrel staves based on short-strip microstrip detectors. The current program of work is aimed at building the next demonstrator stave in 2010.

1.2 The Detector Stave Concept

The mechanics of a stave are a carbon foam core with embedded cooling pipes and carbon fibre facings. Details can be found in [2]. Onto each facing is glued a bus cable, with traces for power and signal distribution. The bus cable also has an electrical shield layer, to prevent injection of signals into the detector from the traces. The detectors are Si microstrips, 100mm by 100mm, each with four columns of 1280 short strips.

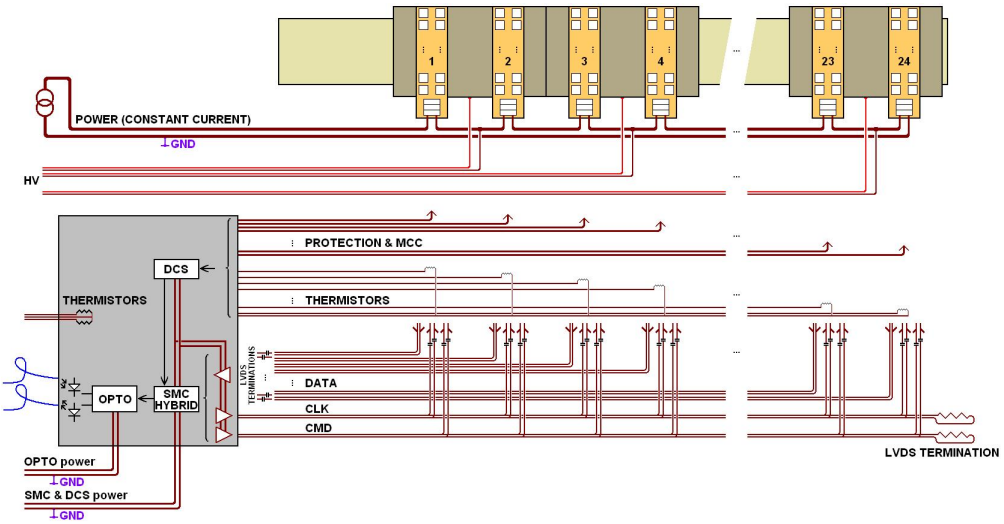

Fig.1 Schematic of a detector supermodule (stave) with serial powering

Fig.1 shows a schematic stave layout. Two readout hybrids per detector are glued directly to the (passivated) silicon detectors. Each hybrid carries two columns of ten ABCN ROICs.

The ABCNs [3] provide greater functionality and speed than ABCDs and will be manufactured in 130nm CMOS (ABCN-13). They are currently prototyped in 250nm CMOS (ABCN-25). The end of stave (EOS) card carries the supermodule controller (SMC), which multiplexes together the data streams from the hybrids and drives an optical transmitter. It also performs the function of decoding timing, trigger and control (TTC) signals recieved via an optical fibre and *p-i-n* diode, and sending them along the bus cable to the readout hybrids.

2.Serial Powering Architecture

2.1 The Serial Powering Concept

For the ATU, an independent LV power cable for each hybrid will not be used. The stave geometry suggests the use of serial powering (SP) [4]. A constant current source supplies 24 hybrids via a single cable chain, reducing the cable count by a factor 24 over independent powering. The current source has been prototyped and used for testing hybrids. Although the concept of serial powering is simple, its practical realisation requires the consideration of a number of complicating factors, which will be outlined here.

2.1.1 Shunt Regulation

The ROICs draw a varying current according to which function they are performing. To keep the hybrid voltage constant and provide a low impedance voltage source, a shunt regulator must be placed in parallel. This may be a separate circuit implemented with discrete components, as has been the case for test staves built so far. More recently, the Serial Powering Interface (SPI) ASIC [5] contains a programmable shunt regulator, programmable linear regulators and LVDS signal buffering. It provides a complete test bed for several SP options.

The use of a stand-alone regulator leads to power dissipation in a small area. Shunt transistors can instead be built within the ROICs. In the ABCN-25, two schemes can be implemented. In one, an external op-amp controls the shunt transistors. In the other, they are controlled by circuitry also within the ROIC.

2.1.2 Analogue and Digital Voltage Supplies

The shunt regulator provides a single voltage, the analogue and digital voltages being derived from it. Table 1 shows the required supplies for the ABCN-25 and ABCN-13.

	analogue V	**analogue I**	**digital V**	**digital I**
ABCN-25 (present)	2.2 V	27 mA	2.5 V	95 mA
ABCN-13 (proposed)	1.2 V	16 mA	0.9 V	51 mA

Table 1 Power consumption of prototype ROICs

In the ABCN-25, the analogue voltage is lower than the digital. Since the analogue current is lower than the digital, the use of an internal linear regulator to derive the analogue voltage wastes little power. For the ABCN-13, the analogue voltage will be higher than the digital and a linear regulator would dissipate significant power. However, this is a conservative solution which is expected not to introduce excess noise. An alternative might be to use switched

capacitor charge pumps to derive the analogue and digital voltages from the shunt voltage, allowing a lower power dissipation.

2.1.3 The Efficiencies of Alternative Powering schemes

We define efficiency as the power consumed by the ABCN-13s on a stave, divided by that delivered by the power supply. Cable losses are important and the supply current must be reduced to minimise them. Assumptions used are shown in Table 2. For the same trace size, the efficiency was calculated for the schemes shown. For IP, the trace width was divided over the 24 modules, resulting in high I^2R losses and very low efficiency. The DC-DC conversion uses 2 stages, from 10V to 1.8V, then to 0.9V for digital and from 10V, to 2.4V, then to 1.2V for analogue. The first stage is a Buck converter (efficiency 85%) and the second a charge pump (efficiency 90%).

We find that a SP design using a linear regulator to derive the digital voltage from the analogue will be more efficient than the DC-DC scheme. This is primarily due to the lower current in a SP chain of 24 modules, cf. DC-DC with gain 11. DC-DC schemes require air-core toroids which must be shielded if they are not to introduce excess noise into the system. A system using SP to give 3.6V followed by charge pumps to derive 1.2V and 0.9V could give a significant efficiency gain over the other two layouts, for the reasons given in Section 2.1.2.

Assumptions used		**Efficiencies of various schemes**	
shunt efficiency	85%	**SP, charge pump**	75%
DCDC efficiency	85% stage 1, 90% stage 2	**SP, linear regulators**	50%
bus Cu trace	0.018mm*7.5mm*1.2m	**DC-DC converters**	40%
long cable R	2 Ohm per pair	**independent power**	1%

Table 2 Power consumption of different schemes, showing assumptions used. The "long cable" is the cable chain from the stave to the power supply

2.1.4 SP Chain Failure Protection

The most damaging potential breakdown of a SP system is that of a hybrid or its connections, in such a way as to break the current loop and cause the whole chain to fail.

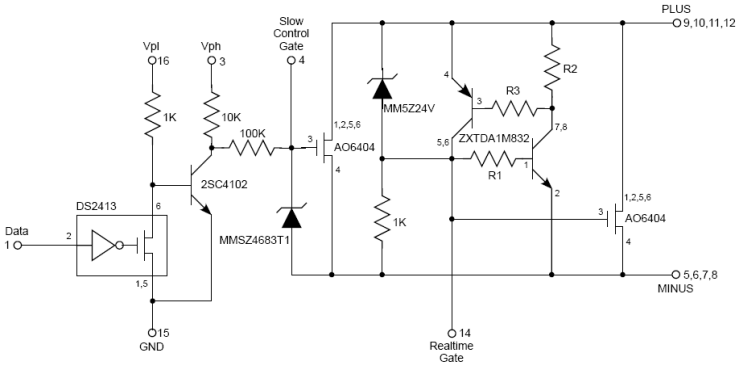

Fig.2 Schematic of SP protection circuit

It is conceptually simple to design a protection circuit to provide a shunt around a failed hybrid, but the realisation is challenging due to power dissipation and small available area.

A circuit is shown in Fig.2 which incorporates two FETs in parallel with each hybrid. One is driven by an external slow control using an addressable switch, whilst the other is connected via a latch to a voltage reference. The latter part of the circuit detects automatically if an open-circuit has occurred and bypasses the hybrid. The protection circuit is ideally placed on the bus cable, to protect against hybrid wire bond breakages. The circuit shown currently uses discrete components, but an ASIC will be designed to implement the same functionality.

2.1.5 High Voltage Supply

Each silicon detector must have a HV supply. This can be achieved using a floating HV supply for each detector, referenced to the current return path of the SP loop, which is referenced to ground at the SCT thermal enclosure. In order to simplify cabling and reduce the amount of material, it is possible to use a single HV cable per stave, as shown in Fig.3. The ground reference is then through the current return path, i.e. through the chain of shunt regulators. These must then have a dynamic impedance which is sufficiently small to avoid introducing excess noise. Noise measurements from this scheme are described in Section 3.1.

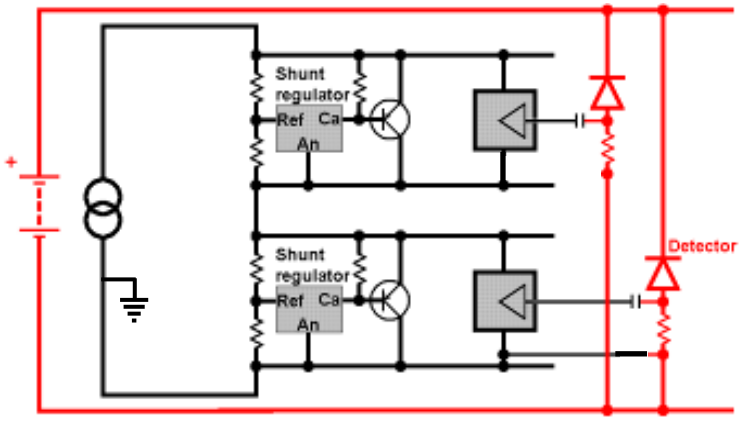

Fig.3 Schematic of single cable per stave HV distribution

2.1.6 Grounding and Shielding

The ground reference of the SP stave is through the current return conductor to a grounding point outside the SCT thermal enclosure. A shielding challenge is that the signal traces on the bus cable should not inject noise into the sensors. The baseline design therefore incorporates an aluminium shield layer in the bus cable. The shield is divided to give a section under each detector, referenced to the SP chain. It is proposed to test several shield designs as part of the current program of work.

2.1.7 Signal Transmission

It is necessary to bring clock and command signals from the SMC to the hybrids and data from the hybrids to the SMC. However, the hybrids all have different potentials with respect to

ground and so all the signals must be ac-coupled. TTC signals are ac coupled at the hybrid and data signals on the EOS card. DC-balanced codes have been proven reliable in this application.

3. Recent Experimental Results

3.1 The 30 module stave

The longest test stave built so far comprised 30 modules, and used ABCD chips. The SP chain carried 0.8A at 120V. This stave verified that: 1) A single HV line per stave can be used. 2) AC-coupled multi-drop LVDS can be used for data and TTC signals. 3) The serially powered stave does not suffer from an increased readout noise level, as shown in Fig.4.

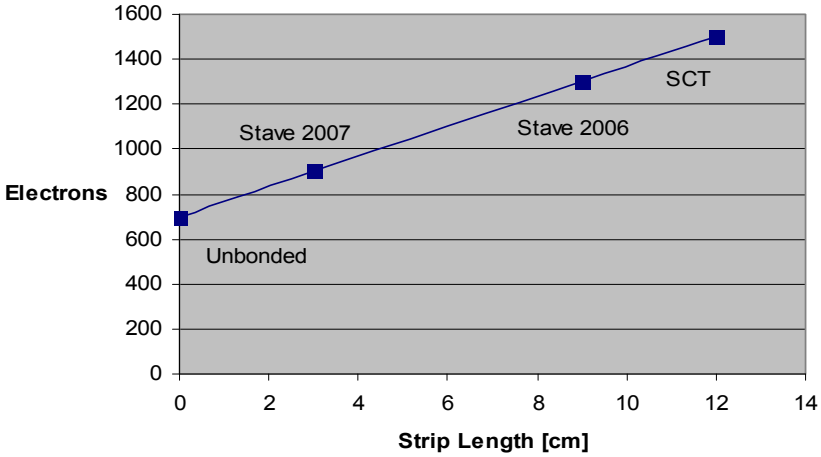

Fig.4 ENC vs strip length when using ABCD chips. Test staves used serial powering. SCT modules and unbonded chips used independent powering.

3.2 Protection circuit

A protection circuit was built as in Fig.2 and tested with dummy loads. In response to a module becoming open circuit, the voltage across it is collapsed in less than 80ns by turning on the relevant FET (Fig.5).

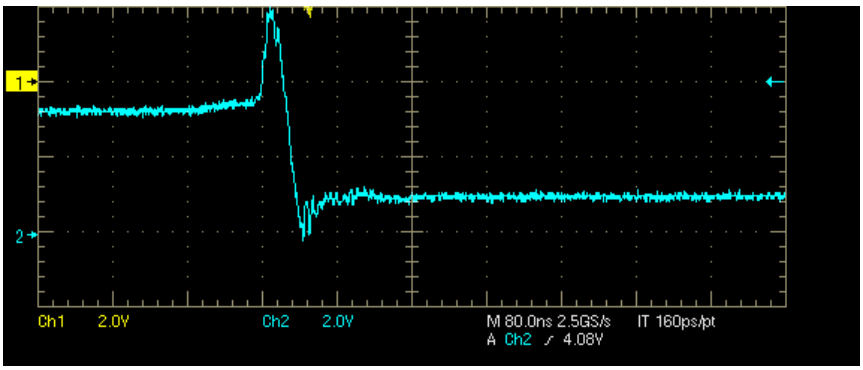

Fig.5 Oscilloscope trace of module voltage being switched off by the protection circuit

Note that the FET under slow control can be connected to an externally derived gate voltage, whilst the real time part of the circuit derives the gate voltage from the module power supply. The former can therefore reduce the module voltage to a lower value than can the latter.

3.3 ABCN-25 SP Options

As described earlier, the ABCN-25 incorporates custom options for SP. A scheme with external regulation of shunt transistors in the ABCN has been tested on single chips and a 20-chip hybrid, using the custom current source. The shunt transistors were controlled by a circuit based on a voltage reference and an op-amp. The ENC was measured as a function of shunt current and is not significantly different from that of the same chip powered from conventional voltage sources, at 380 electrons RMS. The noise performance of the ABCN is improved over that of the ABCD.

Shunt regulation with internal control and internal shunts was tested on a 20-chip hybrid. The ENC was found to be near 450 electrons RMS. This appears to be slightly higher than with the former scheme; however the temperature of the hybrid was not well controlled in this preliminary test.

3.4 SPI chip

The SPI chip was bump-bonded to a daughter PCB. The daughter PCB was connected to a test motherboard which carried the necessary power supplies and signal buffering.

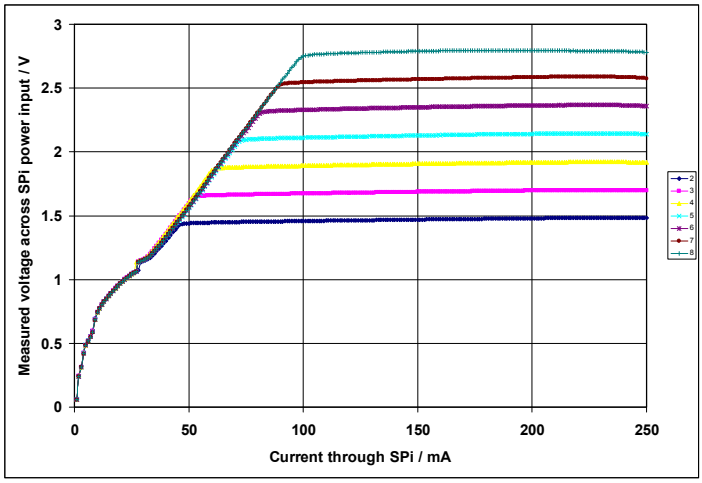

Fig.6 SPI output voltage as a function of shunt current, for different output settings

The SPI was tested for basic functionality: 1) Operation of the serial interface. 2) Ability to read the ADC giving the monitored voltage across the device. 3) Ability to set the voltage using the programmable shunt regulator. Preliminary work has been carried out with the SPI chip used as an external regulator with a 20-chip hybrid. Fig.6 shows that the SPI works well as a shunt regulator, keeping the programmed voltage constant as the shunt current is varied.

4. Future Work

By the end of 2010, it is proposed to build and test a stave which is a realistic prototype for the upgraded SCT. This will be instrumented with 12 detectors and 24 hybrids per side. In late 2009 / early 2010, it is proposed to build test stavelets, which will be single-sided, with up to 8 hybrids. The stavelets will be used with different bus cable designs to select a shielding layout for the full stave. In addition, the SP regulation will be implemented on a plug-in PCB, so that one stavelet may be used for testing several different SP options before making a choice for the full stave. We also intend to test DC-DC converters, provided to us by the DC-DC community, in order to evaluate their performance on the stavelets.

5. Conclusions

Serial powering has been investigated for use in the SCT Upgrade. Simple calculations show that independent powering is not a practical option, due to cable volume and power losses, and that SP can be even more efficient than the presently proposed DC-DC solutions. Nor does SP carry the risk of radiated noise which exists with Buck converters. The most efficient solution could be a SP chain, supplying switched-capacitor charge pumps, which derive the ROIC analogue and digital voltages. Each part in a SP architecture has been demonstrated to work in the laboratory and we are now moving from the use of discrete components to custom ASICs. It remains to build a representative stave with the present generation of prototype ROICs and this is planned for the coming year.

6. Acknowledgements

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