

Determination of Si wafer resistivity distributions by C-V measurements

A. J. Kordyasz^{*†}

Heavy Ion Laboratory, Warsaw University, ul. Pasteura 5a, 02-093 Warszawa, Poland

E-mail: kord@slcj.uw.edu.pl

M. Kowalczyk

Heavy Ion Laboratory, Warsaw University, ul. Pasteura 5a, 02-093 Warszawa, Poland

Institute of Experimental Physics, University of Warsaw, Warsaw, Poland

E-mail: mkk@npdaxp.uw.edu.pl

A. Bednarek

Heavy Ion Laboratory, Warsaw University, ul. Pasteura 5a, 02-093 Warszawa

E-mail: bednarek@slcj.uw.edu.pl

L. Bardelli

University of Florence

I. N. F. N. Sezione di Firenze, Italy

E-mail: bardelli@fi.infn.it

R. Bougault

LPC Caen, ENSICAEN, Université de Caen, CNRS/IN2P3

E-mail: bougault@lpccaen.in2p3.fr

L. Lavergne

Institute de Physique Nucléaire, CNRS/IN2P3. Université Paris-Sud 11

E-mail: lavergne@ipno.in2p3.fr

J. Sarnecki

Institute of Electronic Materials Technology, Warsaw, Poland

E-mail: jerzy.sarnecki@itme.edu.pl

M. Kisieliński

Soltan Institute for Nuclear Studies, Świerk, Poland

E-mail: m.kisielinski@ipj.gov.pl

A. Brzozowski

Institute of Electron Technology, Warsaw, Poland

E-mail: andrzej.brzozowski@itme.edu.pl

K. Pytel

Institute of Atomic Energy POLATOM, Otwock-Świerk, Poland

E-mail: k.pytel@cyf.gov.pl

M. Tarchalski

Institute of Atomic Energy POLATOM, Otwock-Świerk, Poland

E-mail: m.tarchalski@cyf.gov.pl

J. Tarasiuk

Institute of Experimental Physics, University of Warsaw, Warsaw, Poland

E-mail: jt@fuw.edu.pl

P. Grabiec

Institute of Electron Technology, Warsaw, Poland

E-mail: grabiec@ite.waw.pl

A. Panas

Institute of Electron Technology, Warsaw, Poland

E-mail: andrzej.panas@ite.waw.pl

A new method of resistivity distribution measurement of silicon wafers mercury probe was developed. It presents an extension of well known C-V measurement method. The capacitance of the locally created Hg-Si Schottky diode junction on the Si wafer was determined by charge injection into charge preamplifier through the tested diode. The known amount of charge was generated by scientific pulse generator. The capacitance and resistivity distributions of the epitaxial n-n⁺ structure, the high resistivity Topsil float zone wafer and the epitaxial n-n⁺ structure with resistivity locally modified by the Selective neutron Transmutation Doping (SnTD) are presented. The new technological approach used for C-V measurement, together with determination of silicon wafer resistivity distribution are presented. The local modification of silicon resistivity by the SnTD is also determined.

9th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors, RD09

September 30-October 2, 2009

Florence, Italy

*Speaker.

†A. J. Kordyasz

1. Introduction

The resistance uniformity of silicon wafers is essential for proper working of silicon detectors. It is especially important for Pulse Shape Discrimination Technique, where single detector signals are used for charge and mass identification. For these reasons we have elaborated a new method of evaluation of silicon wafer resistivity distribution using the C-V measurements. The method is based on charge injection from scientific pulse generator through tested, biased Hg-Si Schottky diode, into the charge preamplifier. The subsequently measured silicon resistivity distribution gives possibility for:

- Selection of silicon wafers parts with constant resistivity (useful for detector production).
- Correction of the silicon wafer resistivity distribution, using the SnTD [3].

In recent years several methods were developed for capacitance measurement: Bridge Method, Resonant method, I-V Method, RF I-V Method, Network analysis method, and Auto Balancing Bridge Method [1]. Thus, for testing of variable capacitance diodes (varactor diode) and investigation of the MOS structures the Auto Balancing Bridge Method and RF I-V Method with reverse bias was applied [1]. Recently, the silicon detector capacitance versus reverse bias potential was determined by using the Resonant Method [2].

2. The Method

The resistivity distribution of Si wafers is measured using C-V method for biased Schottky diodes formed by Mercury drop gravitationally pressed to the tested silicon surface [4, 5]. The Mercury probe is presented in Fig. 1. In order to allow measurements in all points of the wafer the probe was moved by the computer system. The electronic scheme for a capacitance measurement is shown in Fig. 2. A constant amount of charge was produced by very stable scientific pulse generator connected to the shielded chamber, using 50 Ω cable terminated by 51 Ω resistor. The 50 kHz pulses from the scientific generator had a following characteristics: negative polarity, amplitude 50 mV, rise time 50 ns and width 0.3 μ s. The capacitance was evaluated by measuring of charge injected through the mercury probe working with reverse bias about -1.5 V into the charge preamplifier followed by the amplifier with time shaping $\tau=0.5 \mu$ s and bipolar output. The amplifier was connected through 12 bits ADC with the acquisition system. At each point on the wafer, the pulses were collected by ADC during 0.25 s. The collected pulse spectrum contained about 10^4 events, corresponding to the number capacitance measurements performed by ADC. The most probable value calculated from the collected spectrum was assumed as an evaluated capacitance value. During one second about two points of the wafer were measured. For calibration procedure the Mercury Schottky diode was replaced by calibrating capacitors, connected in series with the calibrating resistance. The calibrating resistance describes of the series resistance of the back contact of the wafer. For a good back contact (very low resistance between evaporated Al and the silicon) the series resistance of the Schottky diode can be neglected and the calibrating resistance is assumed to zero. From capacitance distribution of silicon wafer the resistivity distribution, ρ [Ω ·cm], can be calculated using formulae for depletion depth (2.1) and junction capacitance (2.2):

$$d[cm] = 5.3 \cdot 10^{-3} \sqrt{\rho(V_o + V)} \quad (2.1)$$

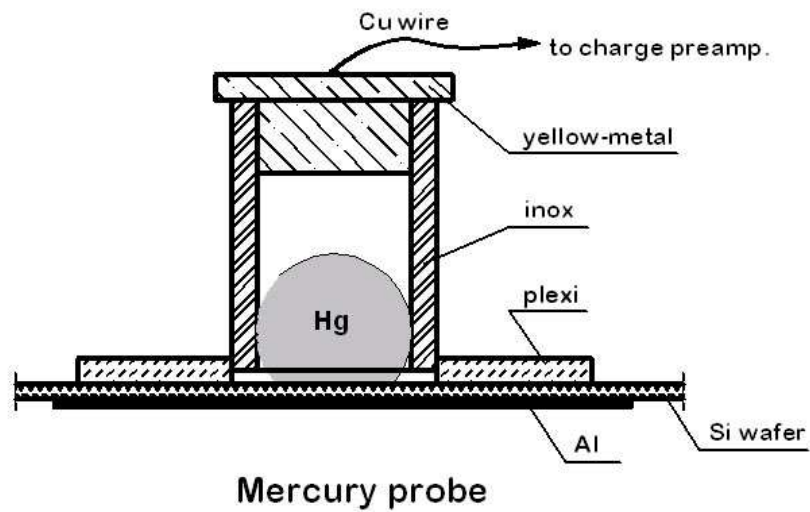


Figure 1: Mercury probe. The Hg drop having diameter 1.3 mm (with circular spot of about 1 mm) was gravitationally pressed to the n-type silicon wafer. To the back side of the wafer with the Al contact is evaporated.

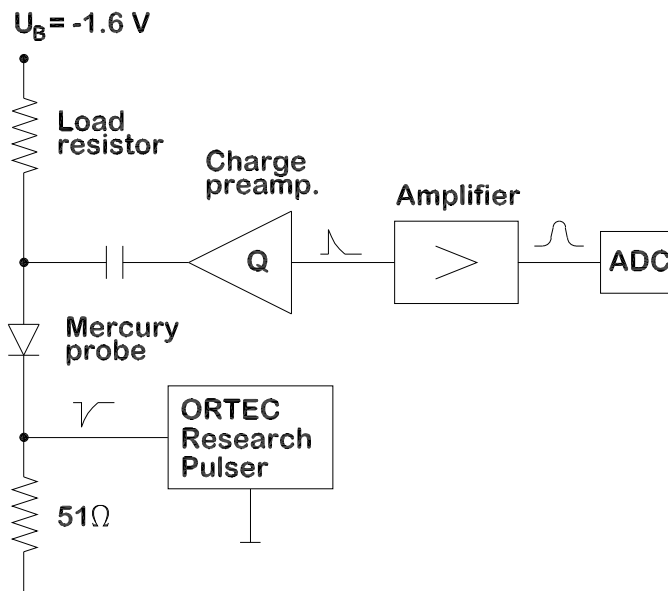


Figure 2: The capacitance of Mercury probe is determined by evaluation of charge injected into the charge preamplifier followed by the amplifier, ADC and acquisition system.

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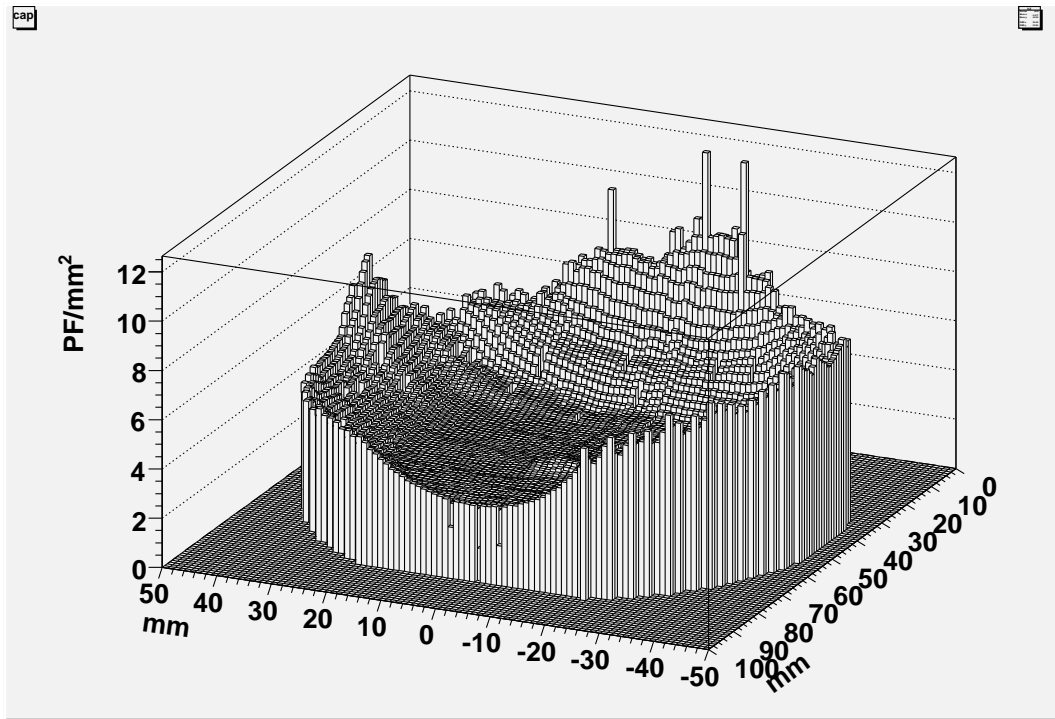


Figure 3: Capacitance [C] distribution. $\langle C \rangle = 2.8 \text{ pF/mm}^2$, $\text{FWHM} = 3.4 \text{ pF/mm}^2$. High resistivity, 4 inches, epitaxial n-n⁺ structure of 118 μm thickness - produced in the Institute of Electronic Materials Technology, Warsaw, Poland.

$$C = 1.17/d \text{ [pF/cm}^2\text{]} \quad (2.2)$$

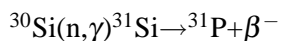
where V_0 and V are the Hg-Si barrier potential and the applied bias potential, respectively.

3. Capacitance and resistivity distributions for the epitaxial n-n⁺ structure and the n-type Topsil wafer

The capacitance distribution of high resistivity epitaxial n-n⁺ structure is presented in Fig. 3. Maximal capacitances are localized at the edges of the wafer. Using formulae (2.1) and (2.2), the resistivity distribution of the wafer can be calculated - see Fig. 4. Due to the enhanced epitaxial edge doping, the resistivity at the wafer edge is considerably reduced. For the Topsil wafer only the resistivity distribution is presented - see Fig. 5. Resistivity distribution of the wafer is uniform, except of the wafer edges where it is mostly increased.

4. Capacitance distribution of the n-n⁺ structure with resistivity distribution modified by the SnTD process

The SnTD [3] is a process in which the silicon wafer resistivity is locally modified by the phosphour donors, produced by the neutron transmutation doping, using the thermal neutron induced capture reaction:



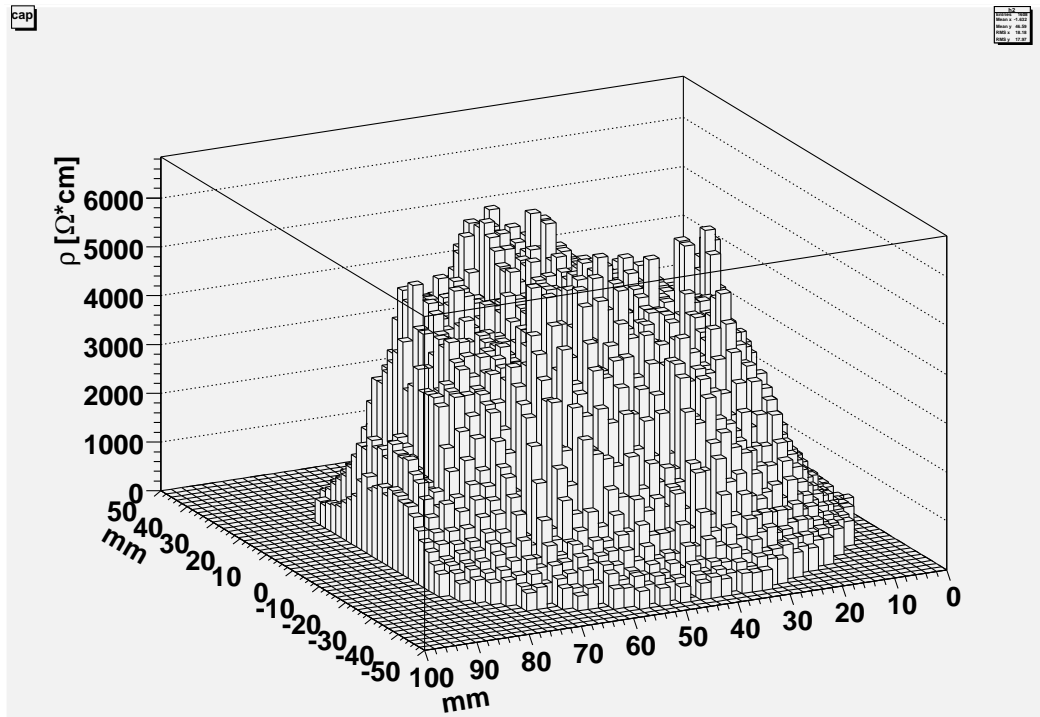


Figure 4: Resistivity [ρ] distribution (2 mm steps). $\langle \rho \rangle = 3.9 \text{ k}\Omega\text{-cm}$, FWHM = 5.5 k $\Omega\text{-cm}$.

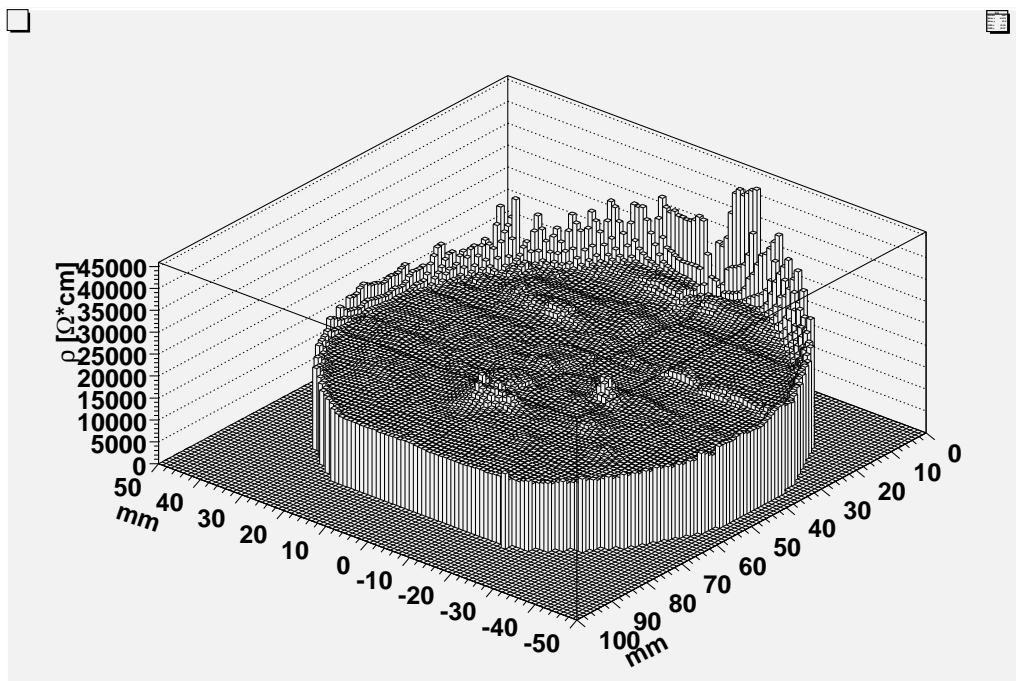


Figure 5: Resistivity [ρ] distribution. Topsisil wafer of 4 inches diameter and resistivity $\rho = 14 - 27 \text{ k}\Omega\text{-cm}$. Series resistance of the back contact is about 130 k Ω . $\langle \rho \rangle = 16 \text{ k}\Omega\text{-cm}$, FWHM = 6.3 k $\Omega\text{-cm}$.

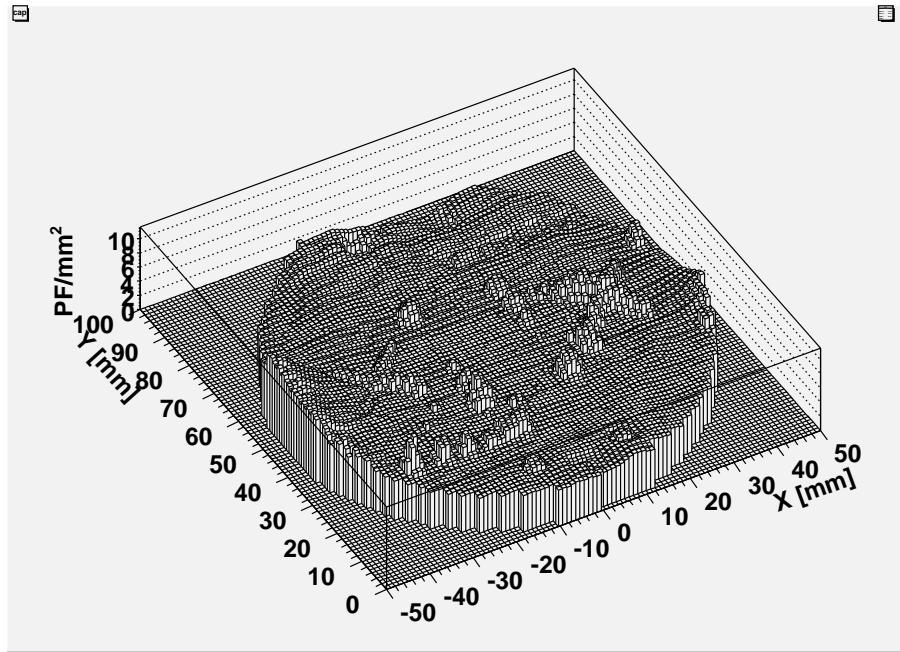


Figure 6: Capacitance distribution of an epitaxial n-n⁺ structure with thickness about 100 μm and resistivity 5000 Ω·cm, after irradiation by thermal neutron flux through the Cd mask of thickness 1 mm with empty holes and two empty crosses. The neutron fluence of about $6 \cdot 10^{16}$ n/cm² was used. The visible “hill structures” correspond to the empty holes and crosses of the Cd mask.

The tested SnTD process was performed by covering four inch high resistivity n-n⁺ structure by 1 mm thick Cd mask with empty holes and two empty crosses. Then mask with n-n⁺ structure was inserted into the thermal neutron flux of about $1.7 \cdot 10^{12}$ n/cm²s, using virtual vertical neutron beam channel of reactor Maria at Świerk in Poland [6]. After irradiation by thermal neutrons, the regions of silicon not covered by Cd mask the silicon have reduced their resistivity. Consequently the measured capacitance increased, what is well illustrated in Fig. 6.

5. Discussion and conclusion

The capacitance of the Hg-Si Schottky junction is not stable - see Fig. 7. In all 8 tested points of the wafer the capacitance dropped about (10-30)% during 140 minutes of measurements. It was probably due to the modification of the silicon by the electric field of the bias potential. To avoid this process we have measured capacitance just after changing of measurement point, with short time of measurement about 0.25 s.

6. Acknowledgements

We would like to thank very much to Krzysztof Rusek, Wojtek Gawlikowicz, Ludwik Pieńkowski, G. Poggi and Daniel Tomaszewski for fruitful discussions and comments.

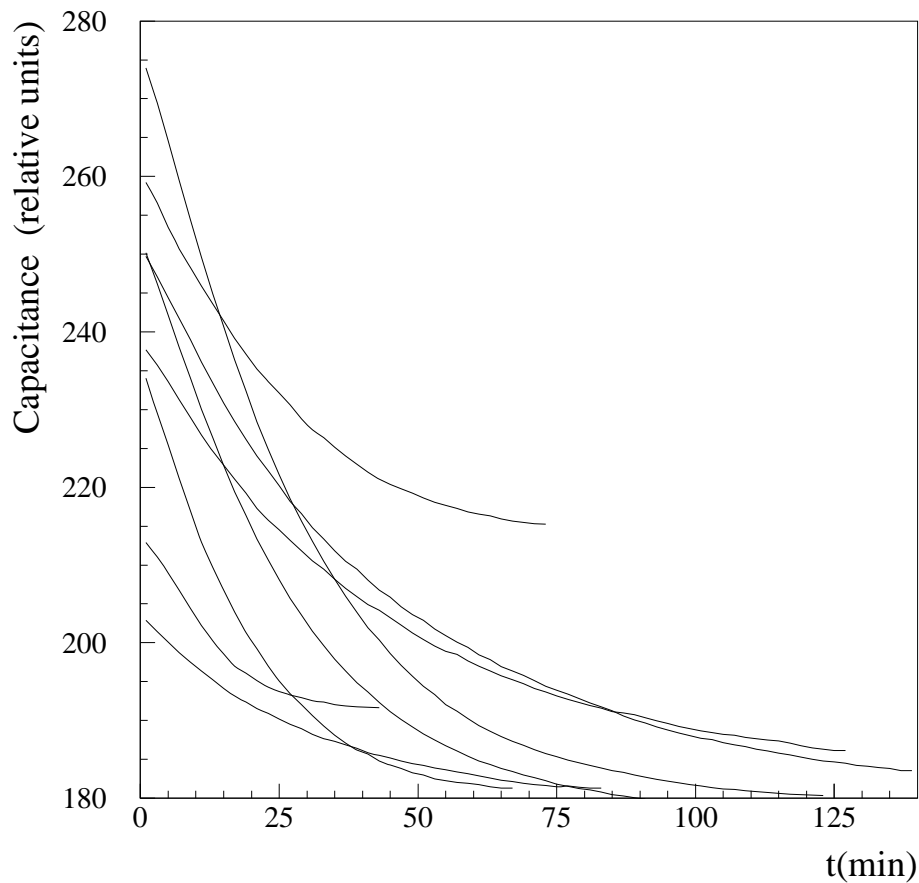


Figure 7: Dependence of Shottky diode capacitance versus time at eight selected points of the wafer.

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