PROCEEDINGS OF SCIENCE

Detectors

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 http://pos.sissa.it/

PoS(LCPS2009)009

Detectors 1: Pixel-based vertex detectors (history). Several important lessons have been learned, and could all too easily be forgotten. Ch D

Detectors 2: ILC detector R&D Ch D

Detectors 3: CLIC detector R&D M H

Detectors 4: Physics and technology of silicon detectors Ch D

Pixel-based vertex detectors – history

(as seen through one pair of eyes)

Chris Damerell (RAL)

All such detectors to date, that have been completed and worked, (only three in fact) have been built by just one evolving detector collaboration. However, very many institutes have participated over the past 30 years …

There are many new detectors of this type in the pipeline, for ATLAS, CMS. ALICE, STAR, SuperBelle, SuperB, …so the story will become more complex

Participating institutions which have made MAJOR contributions:

- Birmingham U
- Bristol U
- Brunel U
- CERN
- Colorado State U
- Edinburgh U
- Lancaster U
- Liverpool U
- U of Massachusetts
- MIT
- MPI Munich
- Nagoya U
- Nijmegen U
- Oregon U
- Oxford U

RAL
SLAC
Tohoku U
UCSB
UCSC
U of Washington
U of Wisconsin
Yale U
and our friends at e2V Technologies

Some of the 'minor' contributions (eg Gary Feldman from Harvard U, Ulie Koetz frm MPI) were nevertheless of critical importance. Each individual (>>100) could give a different and in some respects more accurate presentation of this complex story …

Test of the 'complete theory of particle physics'

- Ch D (post-doc) to Rutherford Lab Scientific Programme Sub-Committee, 2 Feb 1970
- Physics motivation: to build a *focusing spectrometer* (pioneered by Dave Ritson and Karl Brown at Fermilab) for the SPS, then under construction, with sufficient momentum resolution to make definitive tests of the Bootstrap Theory of Strong Interactions (claimed at the time to be the complete theory of particle physics)

Liquid-filled Wire Chambers

Because of diffusion effects (and other effects dependent on the mode of use) gas filled chambers (spark chambers or proportional wire chambers) are limited in resolution to a few tenths of a millimetre.

The Alvarez group has recently[2] observed electron multiplication in liquid argon. This opens the way for an improvement in precision of 2 orders of magnitude; resolution of ~5μ becomes a reasonable possibility.

- By 1974, there were growing doubts about the bootstrap theory. Furthermore it was clear that we could not muster the necessary resources, so we teamed up with the CERN-Munich Group and a more modest goal: to 'think what we could do with their existing PS spectrometer'
- All thoughts of high-precision tracking detectors were shelved, for the time being …
- Thus ACCMOR, one of the most productive collaborations in particle physics, was born
- Meanwhile, events elsewhere (Bell Labs and SLAC) were shaping our future

Invention of the charge-coupled device (CCD)

Charge Coupled Semiconductor Devices

By W. S. BOYLE and G. E. SMITH

(Manuscript received January 29, 1970)

In this paper we describe a new semiconductor device concept. Basically, it consists of storing charge in potential wells created at the surface of a semiconductor and moving the charge (representing information) over the surface by moving the potential minima. We discuss schemes for creating, transferring, and detecting the presence or absence of the charge.

In particular, we consider minority carrier charge storage at the Si-SiO_2 interface of a MOS capacitor. This charge may be transferred to a closely adjacent capacitor on the same substrate by appropriate manipulation of electrode potentials. Examples of possible applications are as a shift register, as an imaging device, as a display device, and in performing logic.

Experimental Verification of the Charge Coupled Device Concept

By G. F. AMELIO, M. F. TOMPSETT and G. E. SMITH

(Manuscript received February 5, 1970)

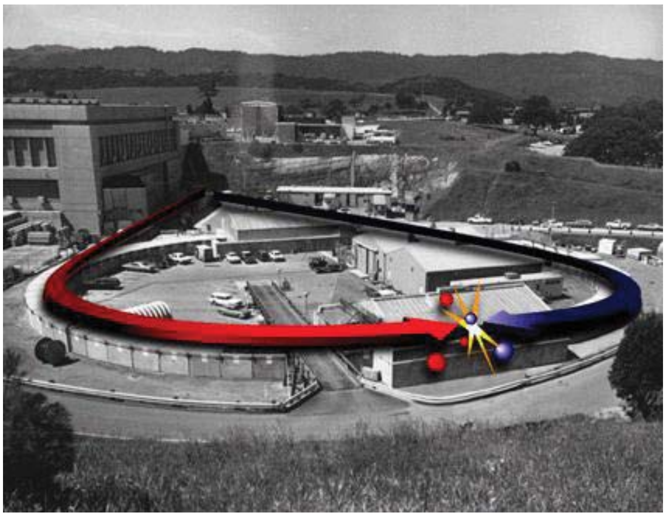
Structures have been fabricated consisting of closely spaced MOS capacitors on an n-type silicon substrate. By forming a depletion region under one of the electrodes, minority carriers (holes) may be stored in the resulting potential well. This charge may then be transferred to an adjacent electrode by proper manipulation of electrode potentials. The assumption that this transfer will take place in reasonable times with a small fractional loss of charge is the basis of the charge coupled devices described in the preceding paper.[1] To test this assumption, devices were fabricated and measurements made. Charge transfer efficiencies greater than 98 percent for transfer times less than 100 nsec were observed.

- **Bell Syst Tech J, 49 (1970) 49**
- **Bell Syst Tech J, 49 (1970) 593**

Boyle and Smith having fun at Bell Labs, 1974

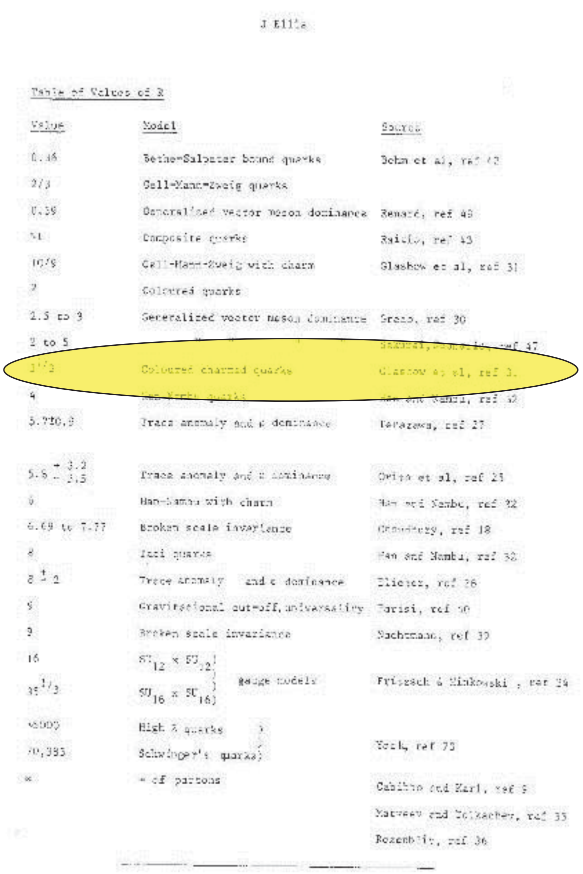
- **but all this passed without notice by the particle physics community**

The discovery of charm



- **SPEAR, an ‘unfunded’ unfashionable minor project, built on a parking lot, started running in 1973**
- **Kjell Johnsen’s visit to SLAC**
- **Purpose? “Measure one number (*R*) then switch it off”**
- **But the first measurements of *R* at high energies (above 3 GeV) were unexpectedly a bit too high ...**

- **ICHEP London July 1974**
- **Burt Richter skipped the ‘boring’ sessions on resonance physics**
- **In his talk, he described the anomalies in experimental measurement of *R*, and John Ellis summarised over 20 possible theoretical interpretations**
- **Returning to SLAC, some of Burt’s colleagues convinced the group to perform a scan at *reduced* energies**



J Ellis

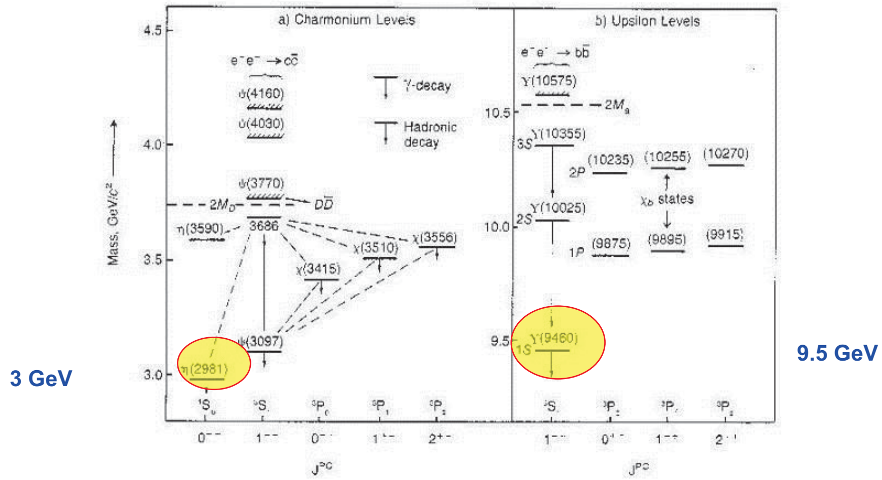
Table of Values of R

Value	Model	Source
0.36	Bethe-Salpeter bound quarks	Bohm et al, ref 42
2/3	Gell-Mann-Zweig quarks	
0.39	Generalized vector meson dominance	Renard, ref 49
[illegible]	Composite quarks	Raitio, ref 43
10/9	Gell-Mann-Zweig with charm	Glashow et al, ref 31
2	Coloured quarks	
2.5 to 3	Generalized vector meson dominance	Greco, ref 30
2 to 5	" " "	Sakurai, Gounaris, ref 47
$3\frac{1}{3}$	Coloured charmed quarks	Glashow et al, ref 3.
4	Han-Nambu quarks	Han and Nambu, ref 32
5.7 ± 0.9	Trace anomaly and ω dominance	Terazawa, ref 27
$5.6^{+3.2}_{-1.5}$	Trace anomaly and ω dominance	Orito et al, ref 25
6	Han-Nambu with charm	Han and Nambu, ref 32
6.69 to 7.77	Broken scale invariance	Choudhury, ref 18
8	Tati quarks	Han and Nambu, ref 32
8 ± 2	Trace anomaly and ε dominance	Eliezer, ref 26
9	Gravitational cut-off, universality	Parisi, ref 40
9	Broken scale invariance	Nachtmann, ref 39
16	$SU_{12} \times SU_{12}$ gauge models	Fritzsch & Minkowski, ref 34
$35\frac{1}{3}$	$SU_{16} \times SU_{16}$ gauge models	
≈500	High Z quarks	Yock, ref 73
70,383	Schwinger's quarks	
∞	∞ of partons	Cabibbo and Karl, ref 9
		Matveev and Tolkachev, ref 33
		Rozenblit, ref 36

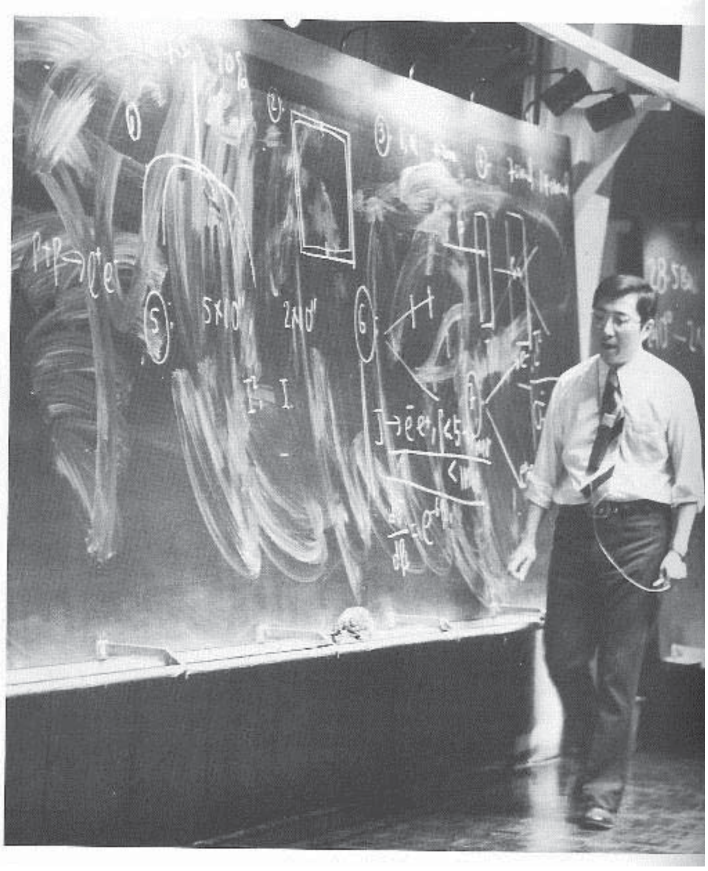
The 'November Revolution' on 10th November 1974 was followed by the Nobel Prize to Richter and Ting in 1976

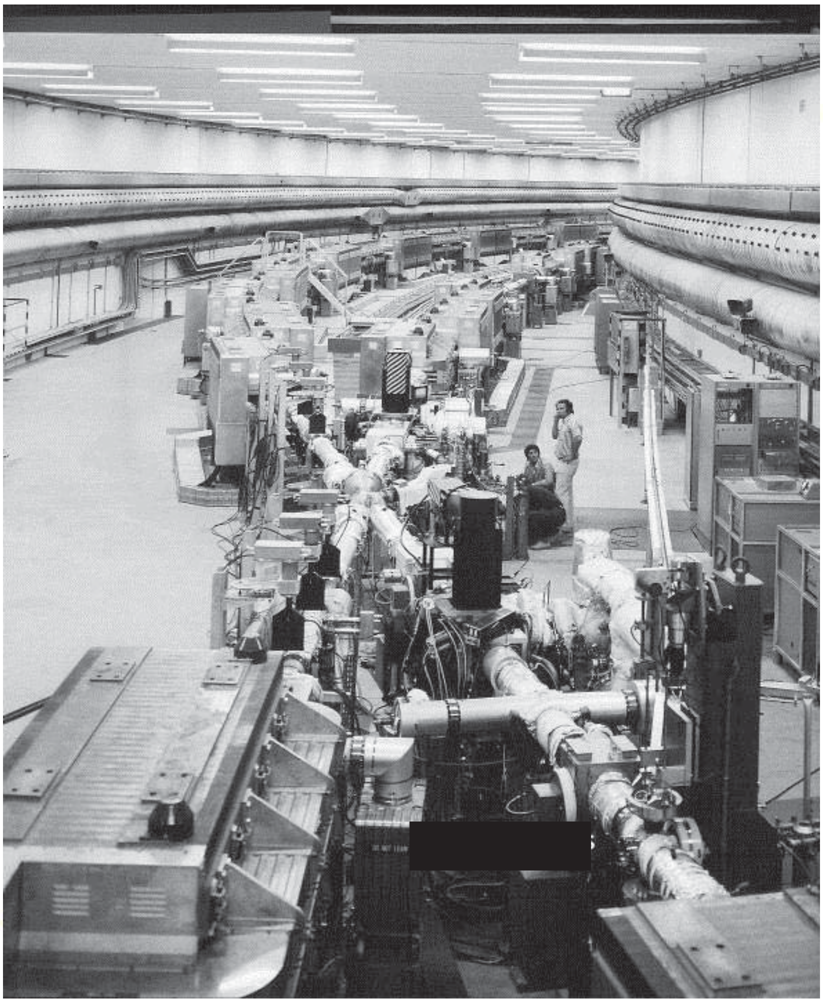
- **PS Committee, Mon Nov 11th 1974. After an hour of theoretical discourse:** ***"Ladies and gentlemen, I have no idea what this discovery means, but it's a disaster for charm"***

- **What had in fact been found was the ground state of charmonium, and the subsequently discovered spectrum satisfied perfectly the expectations of the *non-relativistic quark model.* The bootstrap theory was dead and buried and Dick Dalitz who had lost 2/3 of his audience at the 1965 ICHEP conference, was in great demand at last!**



Look at the masses, remembering that the baryon resonances had completely run out by ~2 GeV. This was extremely unexpected. The upsilon (b-bbar) was discovered in 1977, but the top quark, at 175 GeV, was tough (found in 1994 at the Tevatron, Fermilab), though in 1984 it had been claimed at 60 GeV (UA1)



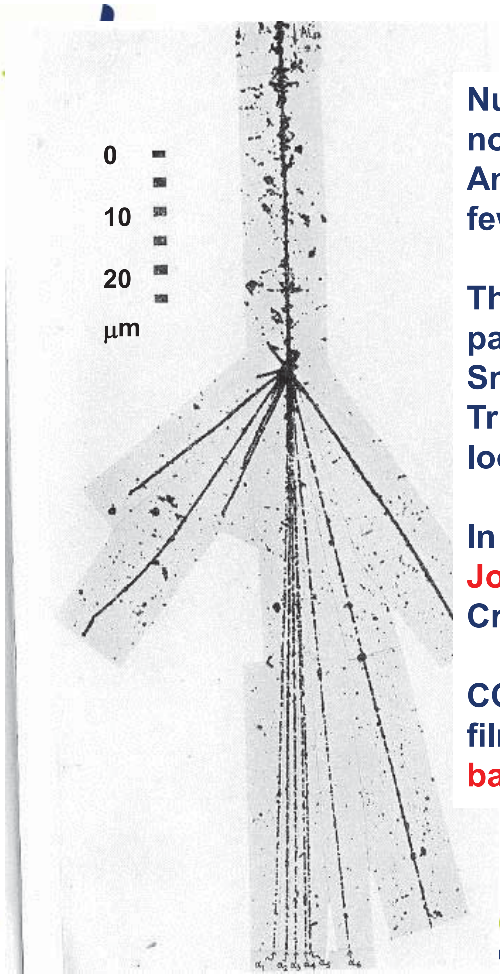


- ISR startup, Jan 1971
- *'The ISR was beginning its reputation as the most perfect machine in high energy physics ever built'*
- So why didn't it discover charm?
- Charmonium was being produced in abundance, but being unexpected, *nobody looked for it*
- [Note: LHC will throw away 99.9995% of their events in the trigger]
- *Tests of the bootstrap theory were much more in vogue*
- CERN had previously turned its back on *another* opportunity to make this discovery
  - The Ting-equivalent proposal had been turned down by the PS Committee in ~1970 as 'crude bump-hunting'

- There followed a small 'commission of inquiry' as to why CERN had missed it …

- Gaillard, Lee and Rosner, 'Search for Charm', Rev Mod Phys 47 (1975) 277, written prior to the events of Nov 10th 1974,

> The shortest track that can be detected in a bubble chamber is a few millimeters. Even at the highest Fermilab energies, one is unlikely to identify a charmed particle of mass greater than about 2 GeV via its track in a bubble chamber. On the other hand, emulsions are sensitive to tracks as short as several tens of microns: one-hundredth
>
> the length detectable in a bubble chamber. Using emulsions, one thus can hope to see charmed particles whose mass is less than about 4 GeV.



Nuclear emulsions, while extremely beautiful, were not appropriate for use in high-rate experiments. An ‘electronic emulsion-equivalent’ detector, with few micron precision, was needed

The CCD invention had been unnoticed by all particle physicists, though Herb Gursky (Harvard-Smithsonian) a member of the Fermilab Board of Trustees, later told me that he had urged them to look at them

In 1978, I was alerted to the possibilities by Jonathan Wright, an astronomy grad student (of Craig McKay) at Cambridge U

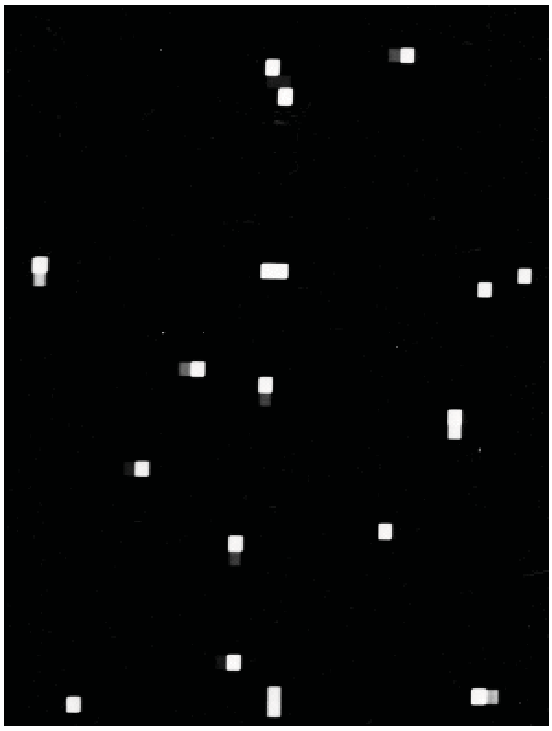
CCDs were beginning to outperform photographic film in astronomy, but suffered from an annoying background due to hits from cosmic rays!

- General reaction in ACCMOR to the Gaillard-Lee-Rosner paper was, how can we make an electronic tracking detector having emulsion-like precision? (what we now call a vertex detector)

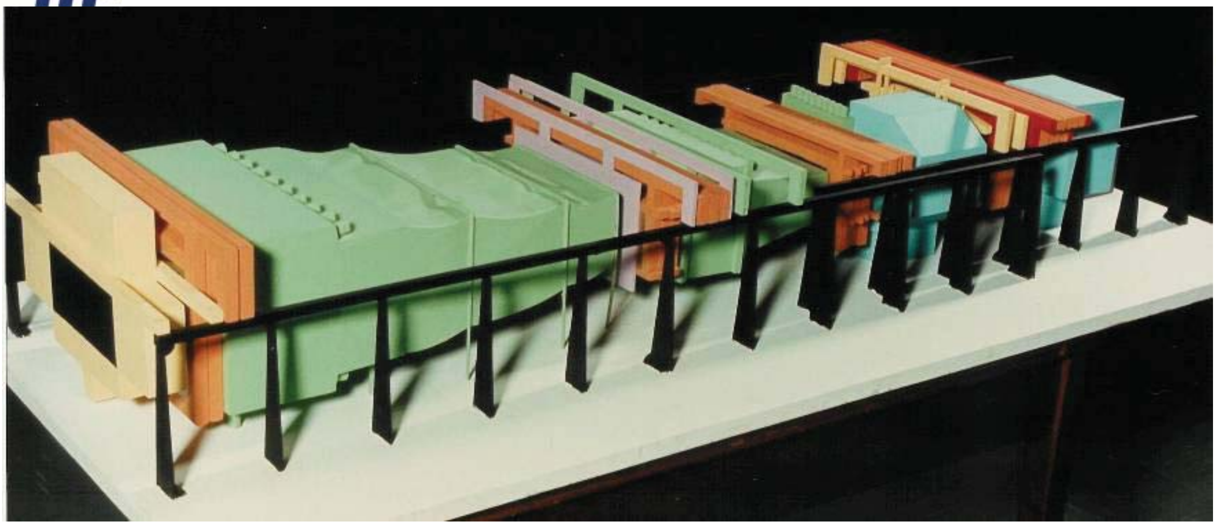
- *This triggered R&D on high pressure drift chambers, silicon microstrips, a silicon drift detector, a silicon active target, and CCDs as tracking detectors*

- With that one exception, we decided to explore condensed matter tracking detectors, and we recognised that the planar technology (‘microelectronics’) should allow *silicon* to leapfrog beyond the potential of say liquid argon or xenon, which had been the front-runners 4 years earlier

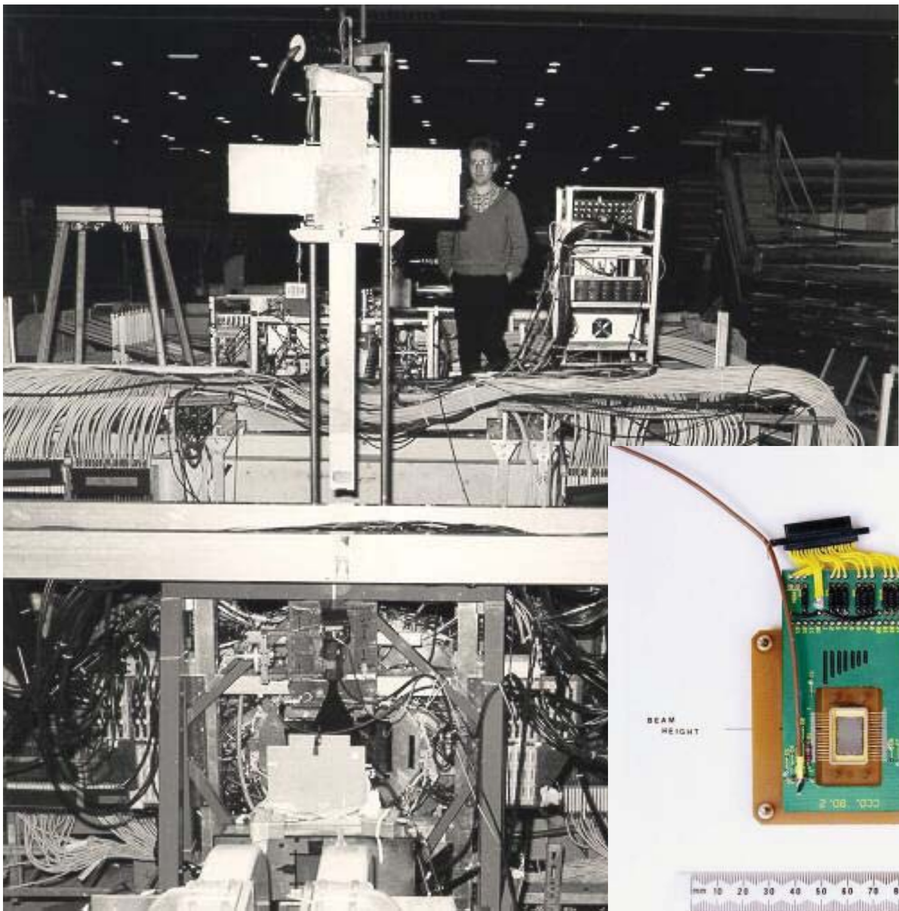
ACCMOR Collab Mtg, Schloss Ringberg, 1980 (Microstrips well-advanced, CCD R&D just beginning)



Steve Watts having fun in the t6 beam, CERN 1980 **1 mm^2 of raw data**



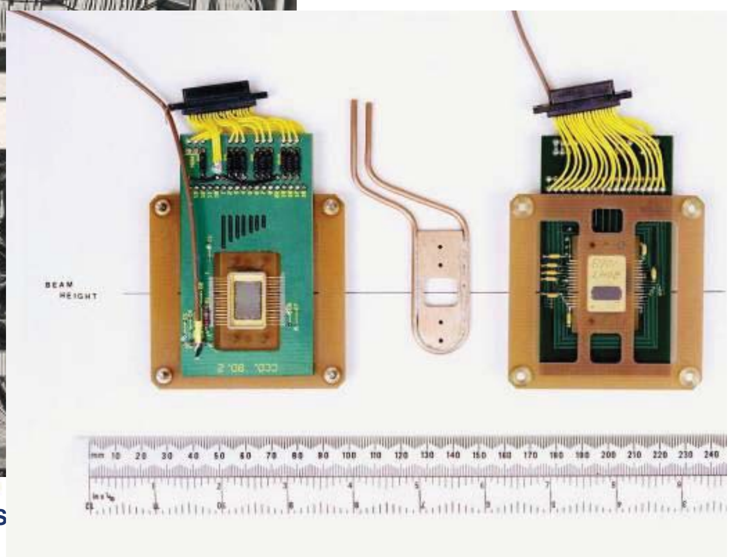
- ACCMOR collaboration had been struggling for years to see charm production at the CERN SPS
- We had built a powerful multi-particle spectrometer, but we lacked a vertex detector of sufficient resolving power
- After 5 years of R&D in the lab and the t6 test beam in the PS East Hall at CERN, the Rutherford group was ready in 1984 to have a go
- Several crates of champagne were eventually ‘won’ as a result



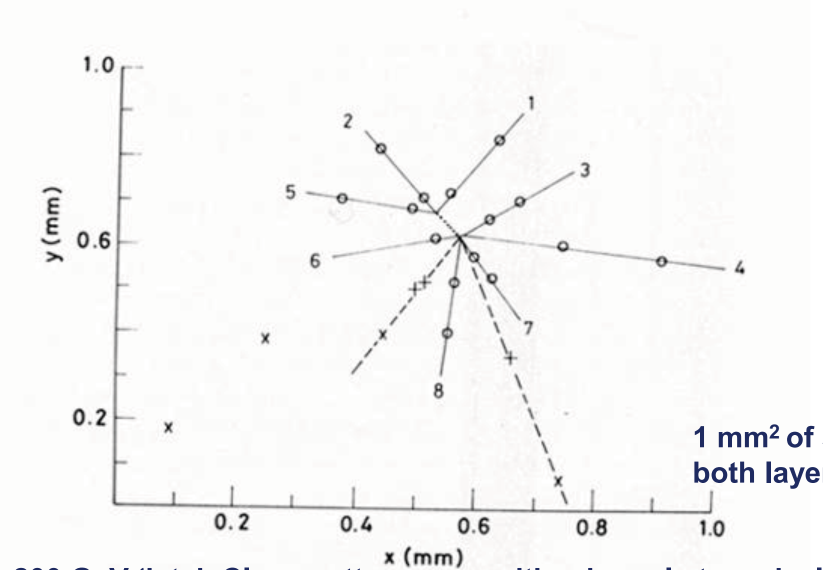
NA32 Experiment

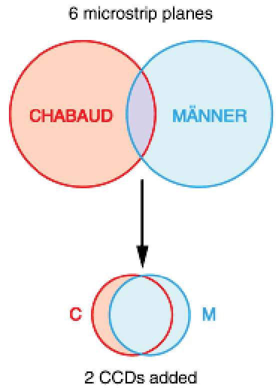
North Hall CERN 1984

Two CCDs, active area 0.5 Mpixels total, 1 and 2 cm beyond the target



A pixel detector provides maximum information per layer, free of ghost hits





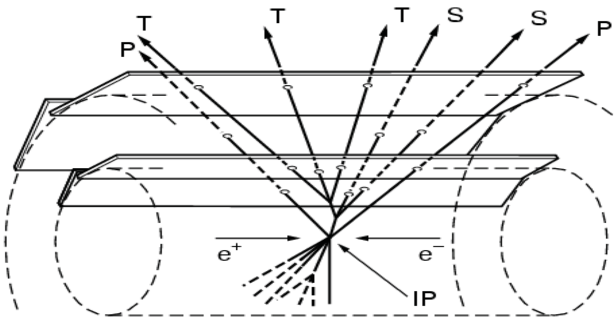
1 mm² of sparsified data, both layers shown together

200 GeV 'jets', Clean pattern recognition by only two pixel planes

Fred Wickens on shift 1984, 'Do you think this looks like a charm decay?'

[After momentum analysis and particle ID, it proved to be our first D^+]

While we had our hands full trying to build a detector with <1 Mpixel, we also had our eyes on the even bigger physics goals associated with the next generation of e+e- colliders, LEP and SLD

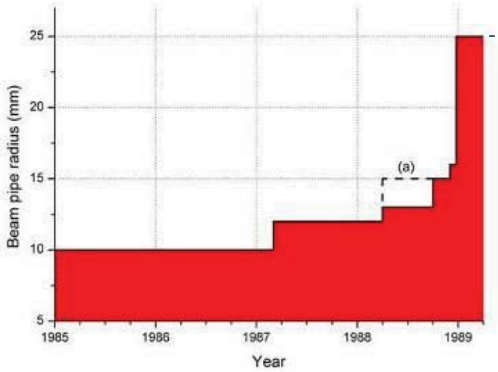


- **Vertex detectors were urgently needed (but not yet working) in the much more challenging collider experiments:**

'Some presently marginal signals (such as the top quark in UA1) could be transformed into definitive experimental results with the aid of vertex detectors …'

Ch D, Proc SLAC Summer Institute 1984, p 45

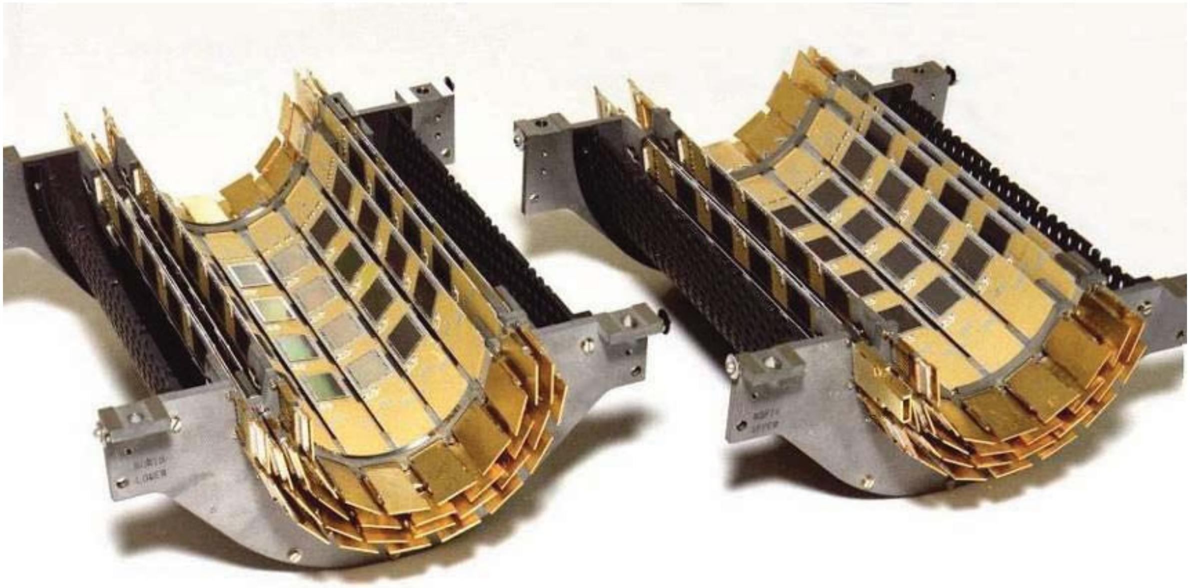
- **Discouraged by the prospects at LEP (Villars workshop June 1981), but encouraged by discussions at the Fermilab workshop on silicon detectors (Ferbel and Kalbfleisch) in October 1981, we decided to join SLD … But what happened to the 'drinking straw'?**



still 4 times better than LEP, at the time

SLD Advisory Gp Mtg Feb 1989: "480 CCDs is ridiculous!"

SLC, another 'good idea' at SLAC, and a 307 Mpixel vertex detector



September 1991

SLD's upgrade vertex detector VXD3:

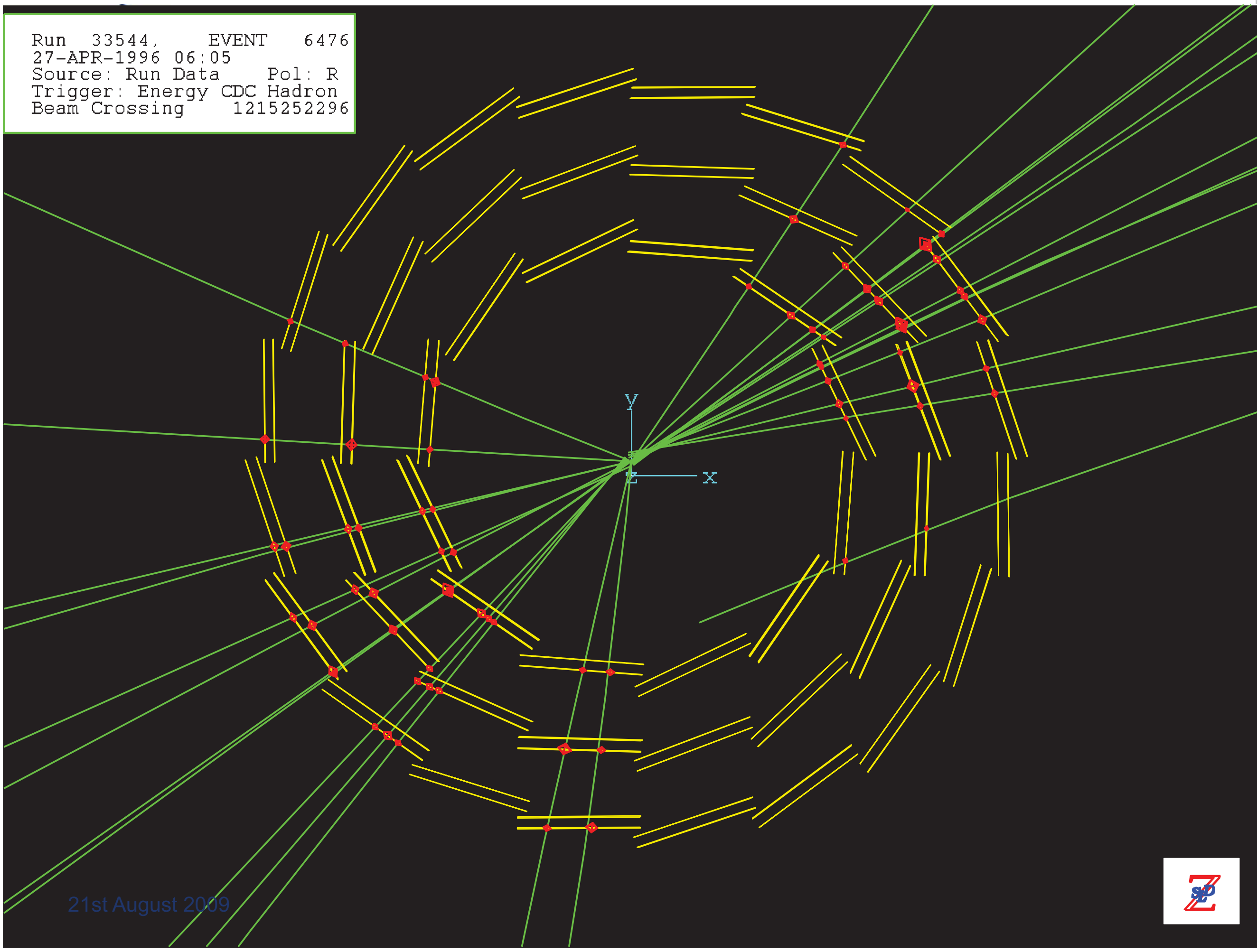
Su Dong: 'That's the vertex detector I joined SLD to build'

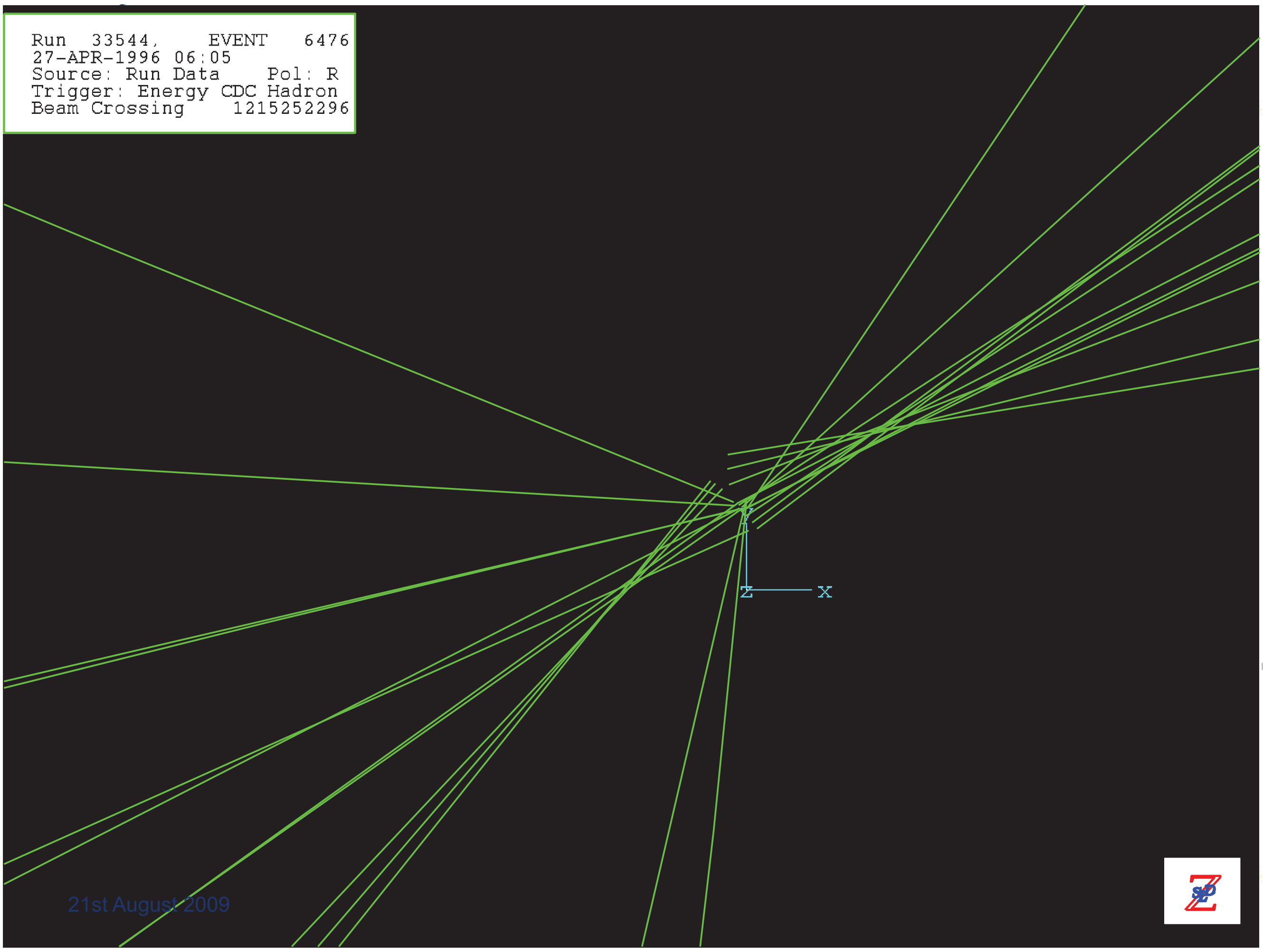
Installed 1995

307 Mpixels

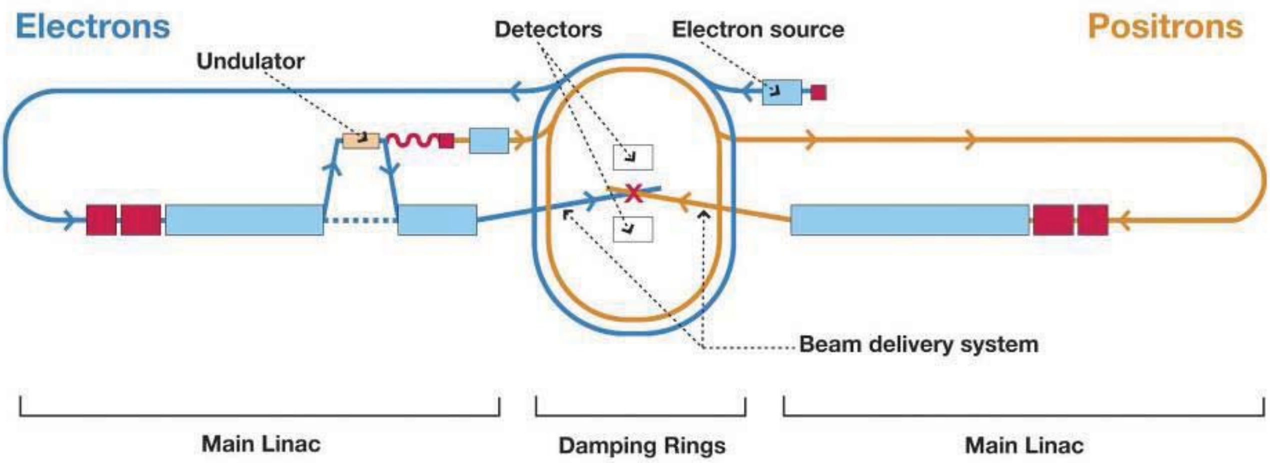
Layer thickness 0.4% X_0

R_{bp} = 25 mm





ILC

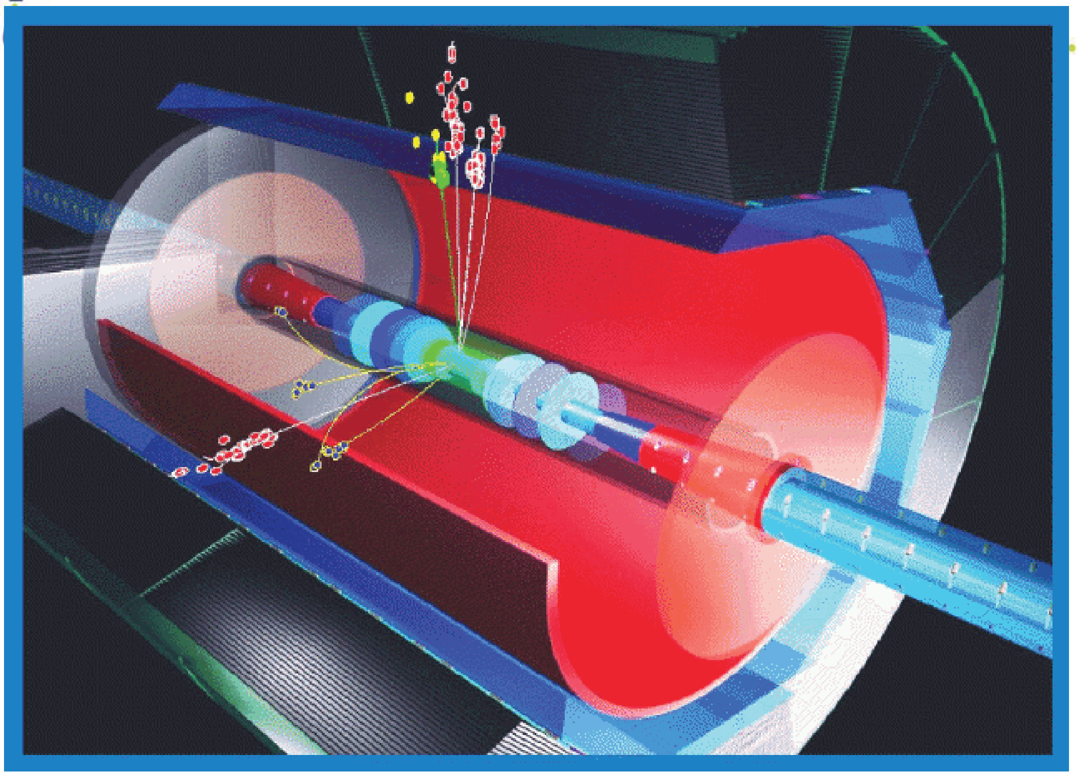


Overall length ~ 35 km, about 10 times SLAC linac in size and energy reach

Each of two detectors may weigh 1-10 ktons, and operate in push-pull mode

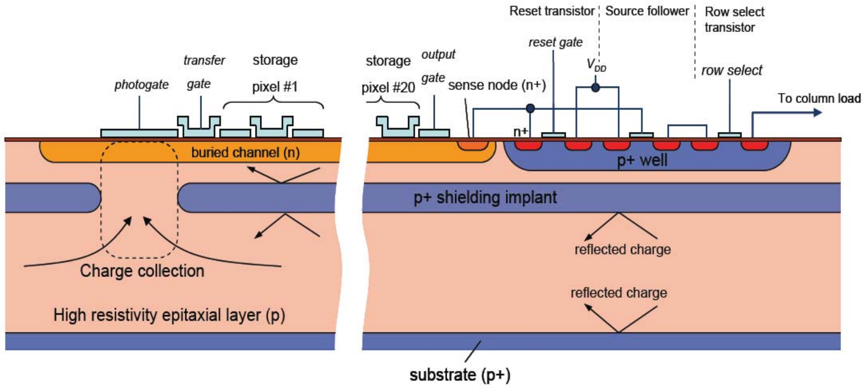
Beam is delivered in 3000-bunch trains of duration 1 ms, every 200 ms

Could be running before 2025, if early LHC results are encouraging, and some country or region bids to host, unless overtaken by CLIC …



- In contrast to the previous (Mark II) vertex detector, the SLD detector was extremely robust, even in sometimes high background conditions. It also easily established the 'world record' for performance (impact parameter precision as fn of momentum) and hence far more physics-per-event than at LEP (1/40 of LEP data, but world's best measurements for charged and neutral *B* lifetimes, R_b, A_{FB} (b) A_{FB} (c), B_d and limit on B_s mixing …
- This led to an explosion in R&D for all sorts of novel pixel sensors that might be used as vertex detectors at ILC. All are monolithic silicon-based
- However, the technology choice is still wide open between ~ 8 options
- Partly related to the broader debate between CCD and CMOS imaging devices (Fossum)
- More on this later today, but let's take a quick look at one option, which is helping to pioneer a new trend in silicon imaging devices …

In-situ Storage Image Sensor (ISIS)



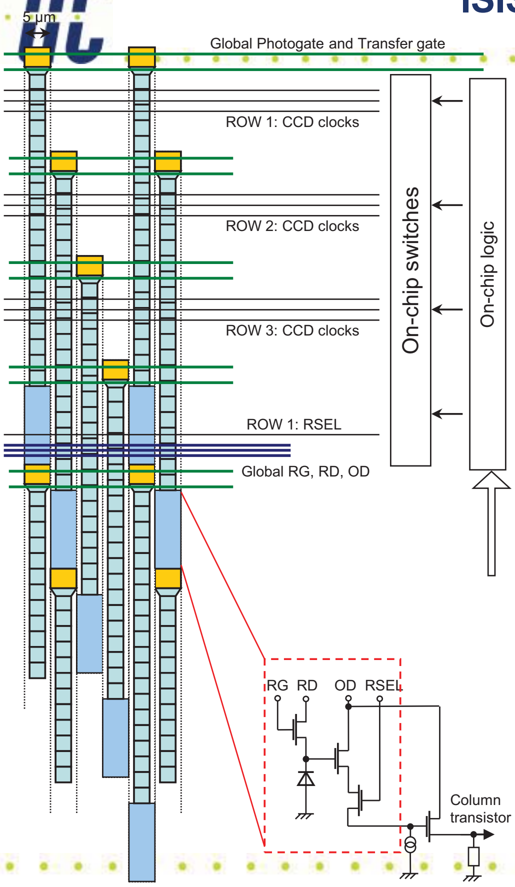
• Beam-related RF pickup is a concern for all sensors converting charge into voltage during the bunch train;

• The In-situ Storage Image Sensor (ISIS) eliminates this source of EMI:

- Charge collected under a photogate
- Charge is transferred to 20-pixel storage CCD in situ, 20 times during the 1 ms-long train
- Conversion to voltage and leisurely readout in the 200 ms-long quiet period after the train, RF pickup is avoided
- 1 MHz column-parallel readout is sufficient

• Output for each bunch train thus comprises 20 frames of low-noise data, and this level of time-slicing will suffice for anticipated ILC backgrounds

ISIS – plan view



• Even more important:

- Entirely avoids need for ‘pulsed power’
- Easier to drive because of the low clock frequency: 20 kHz during capture, 1 MHz during readout
- ~100 times more radiation hard than conventional CCDs – far fewer charge transfers

• ISIS combines CCDs with CMOS in one device: a member of the new family of ‘charge-coupled CMOS’ pixels [Sunday’s talk]

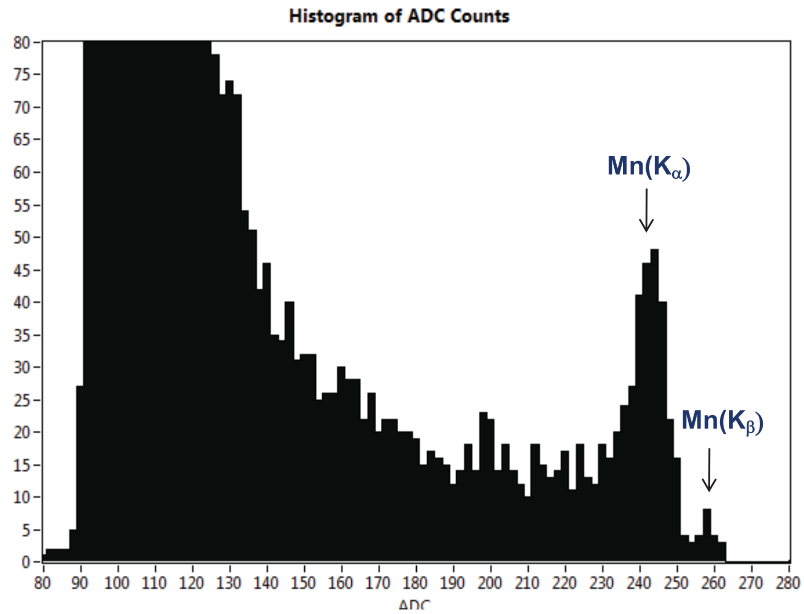
• “Proof of principle” device (ISIS1) designed and manufactured by e2V Technologies, tested successfully at RAL last year

• Prototype in 0.18 μm CMOS (ISIS2) designed at RAL and manufactured at Jazz Semiconductors, now under test at RAL and Oxford U

^{55}Fe signal on test structure - Gary Zhang – 4 June

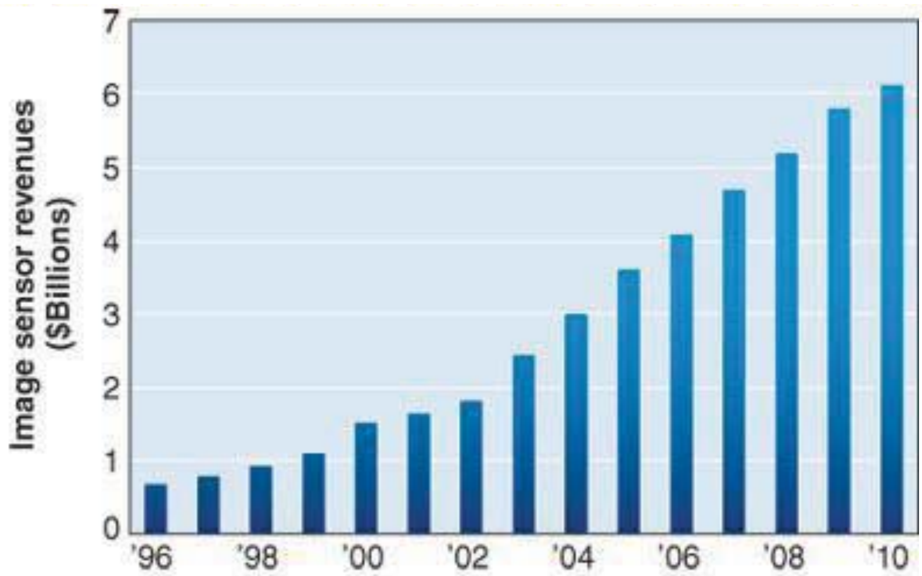
Hits on
O/P node

~6 (μm)^2



ADC counts, ~12 e-/count

- Such energy resolution never seen in CCD-based vertex detectors. Secret is mainly the responsivity of the output node: 24 μV/e- compared with about 3 μV/e- with CCDs
- Shaping time matched to 7 MHz readout; rms noise 5.5 e-
- Promises micron precision in centroid finding for MIPs with ~normal incidence



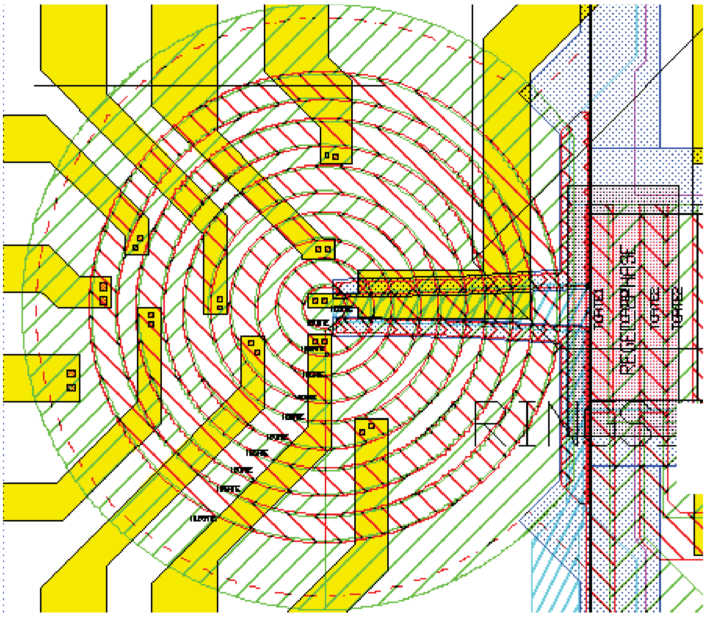
“There is one thing stronger than all the armies in the world; and that is an idea whose time has come”

Conclusions

- From small beginnings 30 years ago, silicon-based pixel detectors have become the 'preferred option' for vertex detectors in particle physics, and are poised to expand into the volume occupied by general tracking detectors, in many cases displacing gaseous and silicon strip detectors
- As well as ILC, there are exciting *near-term* applications at 4th generation SR sources (LCLS and XFEL); fast-frame X-ray cameras for molecular biology and other fields
- The rapid evolution of charge coupled CMOS pixels provides an 'enabling technology' which will enhance the prospects for ILC vertexing and tracking (for the latter topic, see next talk)
- An opinion in one of the LOI groups is that 'the better is the enemy of the good', but when there's time to develop the better, why not go for it?

Backup

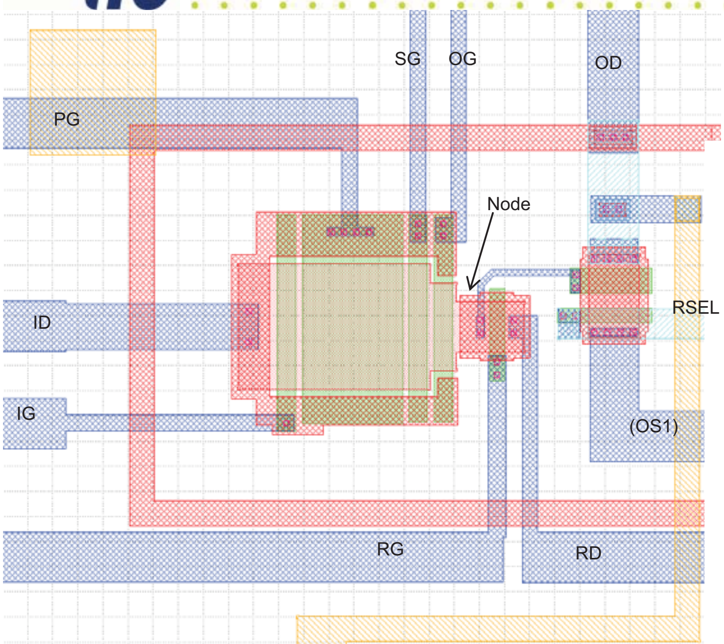
- It turns out that both funnel and register have been fabricated by e2V for confocal microscopy: 100% efficient for single photoelectrons – noiseless, by using LLL (L3) linear register

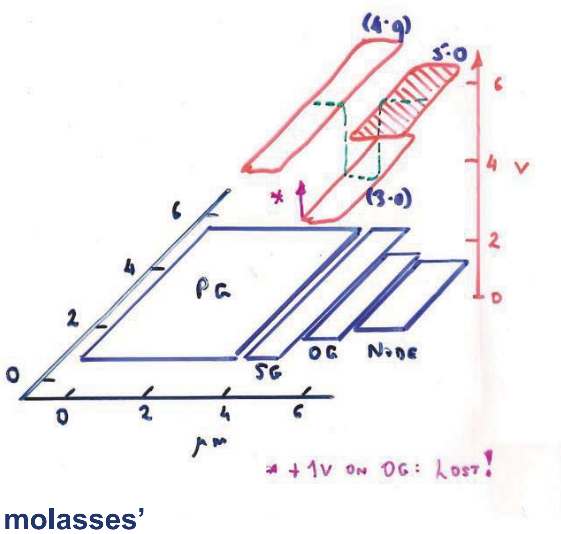


Diameter of outer active ring ~ 100 μm

[David Burt, e2V technologies]

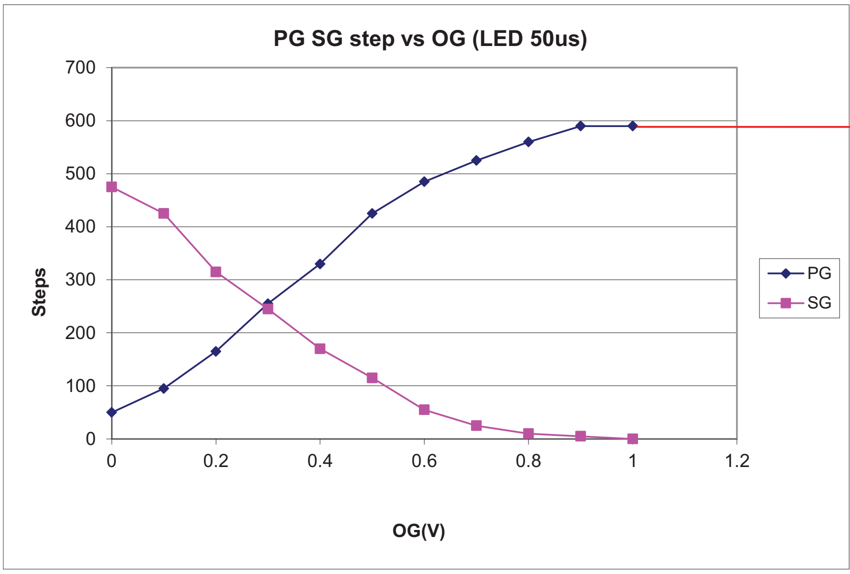
ISIS2 test structure – short CCD





Polysilicon gates (undoped, no silicide) are 'slow as molasses'

Short-channel and fringing field effects are large. Former have been simulated, latter not yet, but we can infer some things from our experimental results …

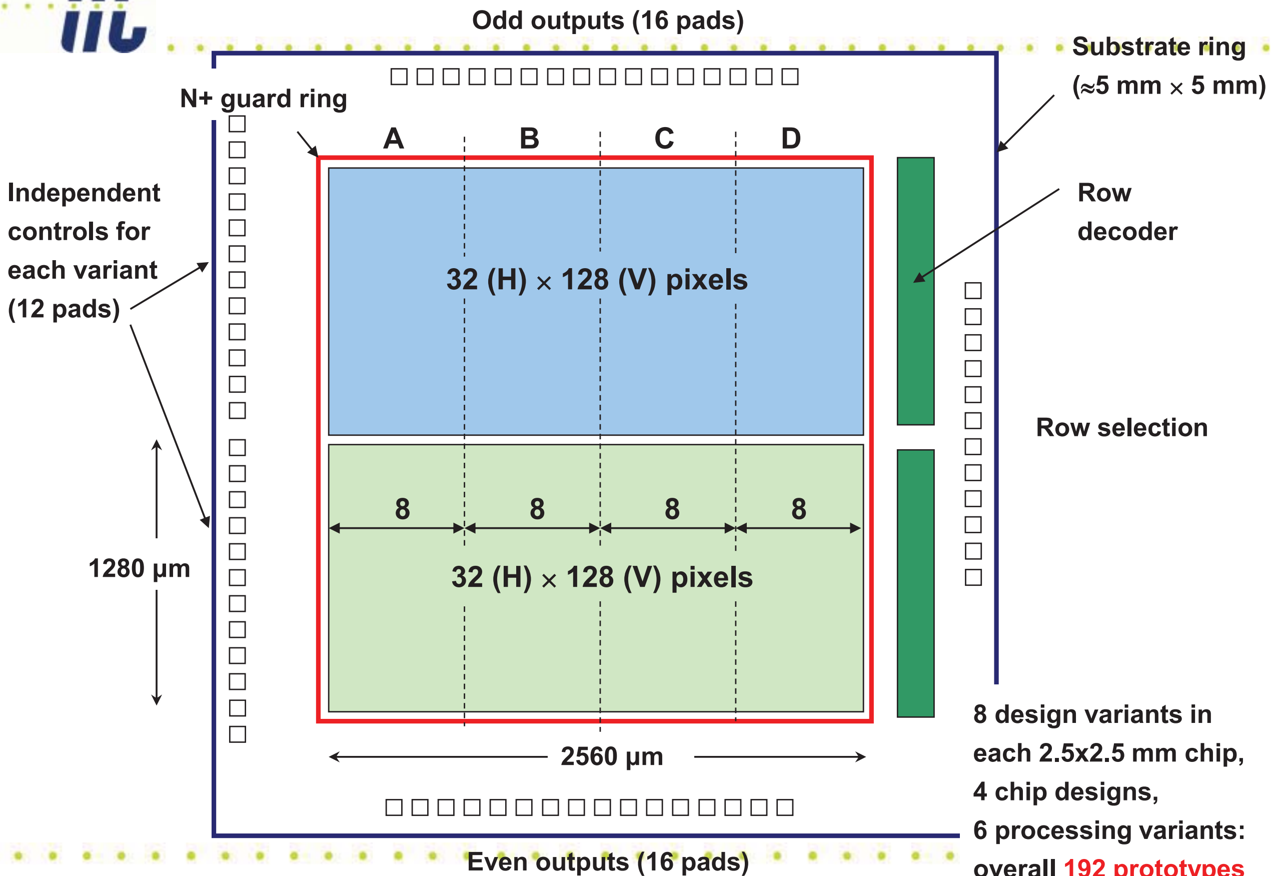


For 2 months, we were effectively at ~2.5 V

Results of 20 Feb 2009

Good performance when VOG = -0.2 V

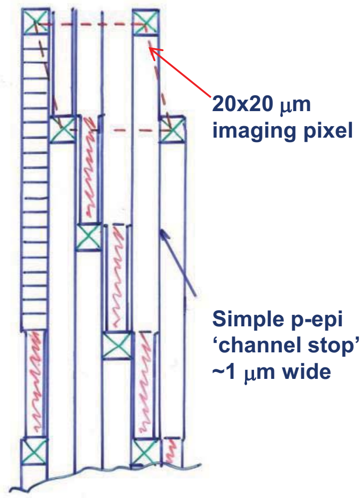
ISIS2 – Chip Layout



8 design variants in each 2.5x2.5 mm chip, 4 chip designs, 6 processing variants: overall 192 prototypes to test. How?

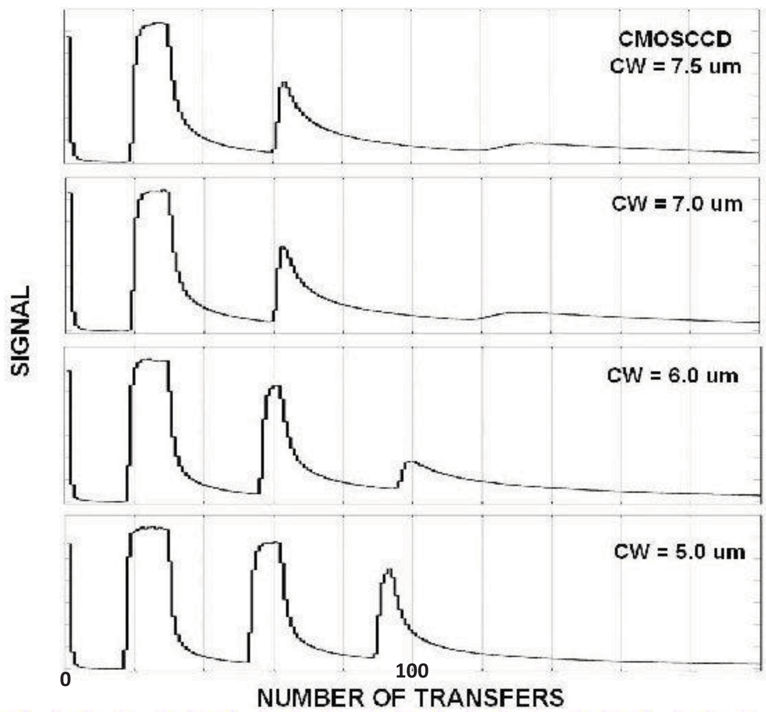
ISIS-3 and beyond

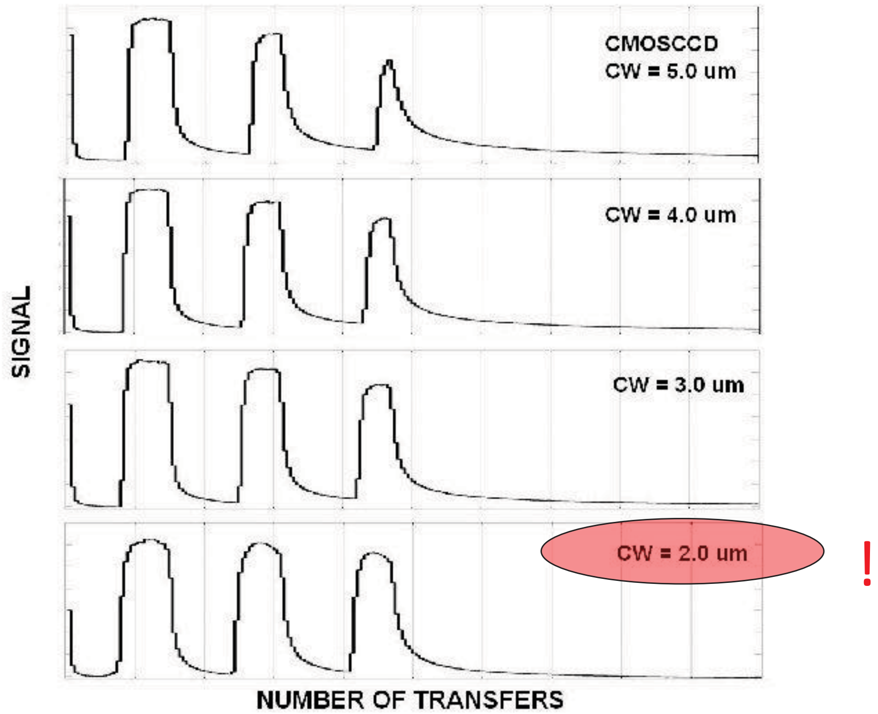
- ISIS-3 could be a relatively inexpensive small-area prototype, incorporating all we learn from ISIS2, and using Jim Janesick's Sandbox facilities
- Once ISIS-3 works, one would want to move to ladder-scale devices, and their assembly into a telescope for evaluation in a high energy test beam circa 2012
- Limited to ~20 time slices with this 0.18 μm technology, but one could double or triple that figure by stacking the devices in a 'vertically integrated' or 3-D structure. One would use tier-1 for time slices 1-20, tier-2 for slices 21-40, etc
- This would preserve the key ISIS selling points of complete freedom from pulsed power, and pickup-immunity during the train



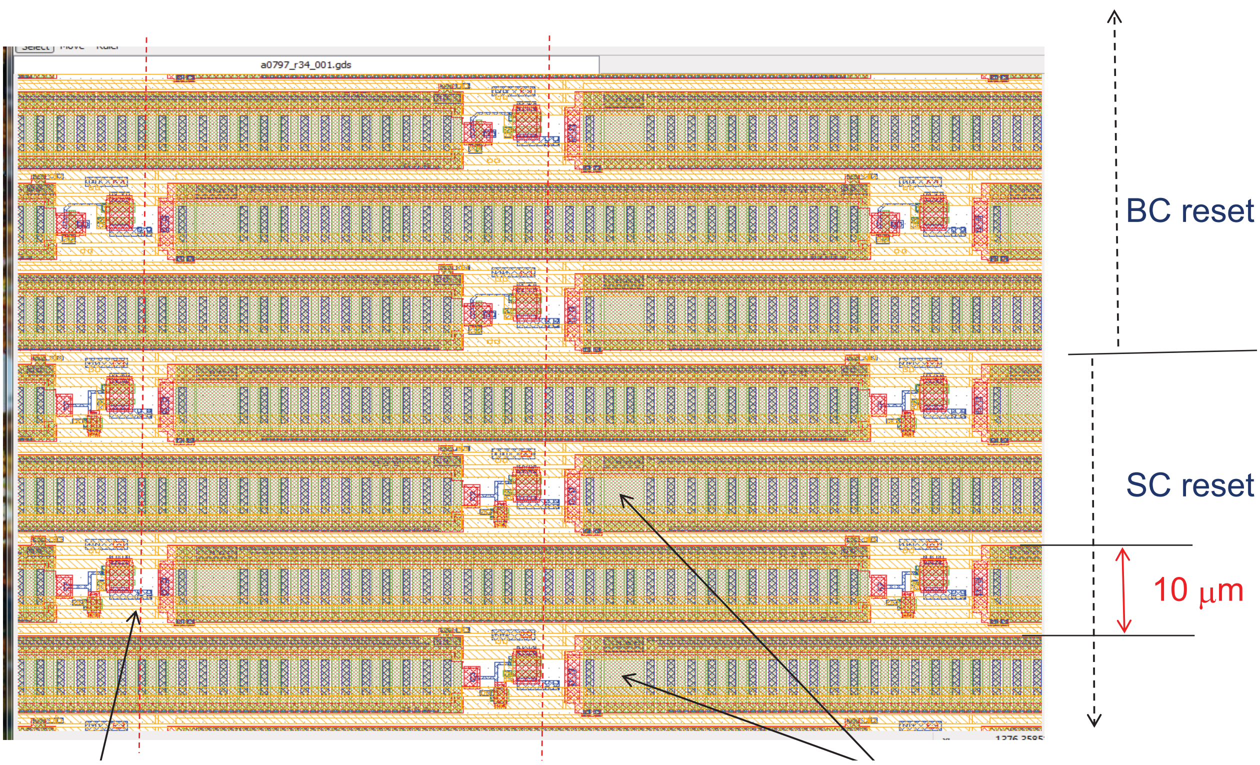
[Assumes the process variation of 'implant before patterning' gates can be exploited to also permit gate connections in the storage register area]

Results from Jim Janesick, December 2008, also working with Jazz Semiconductors





ISIS-2 - pixel layout in main array



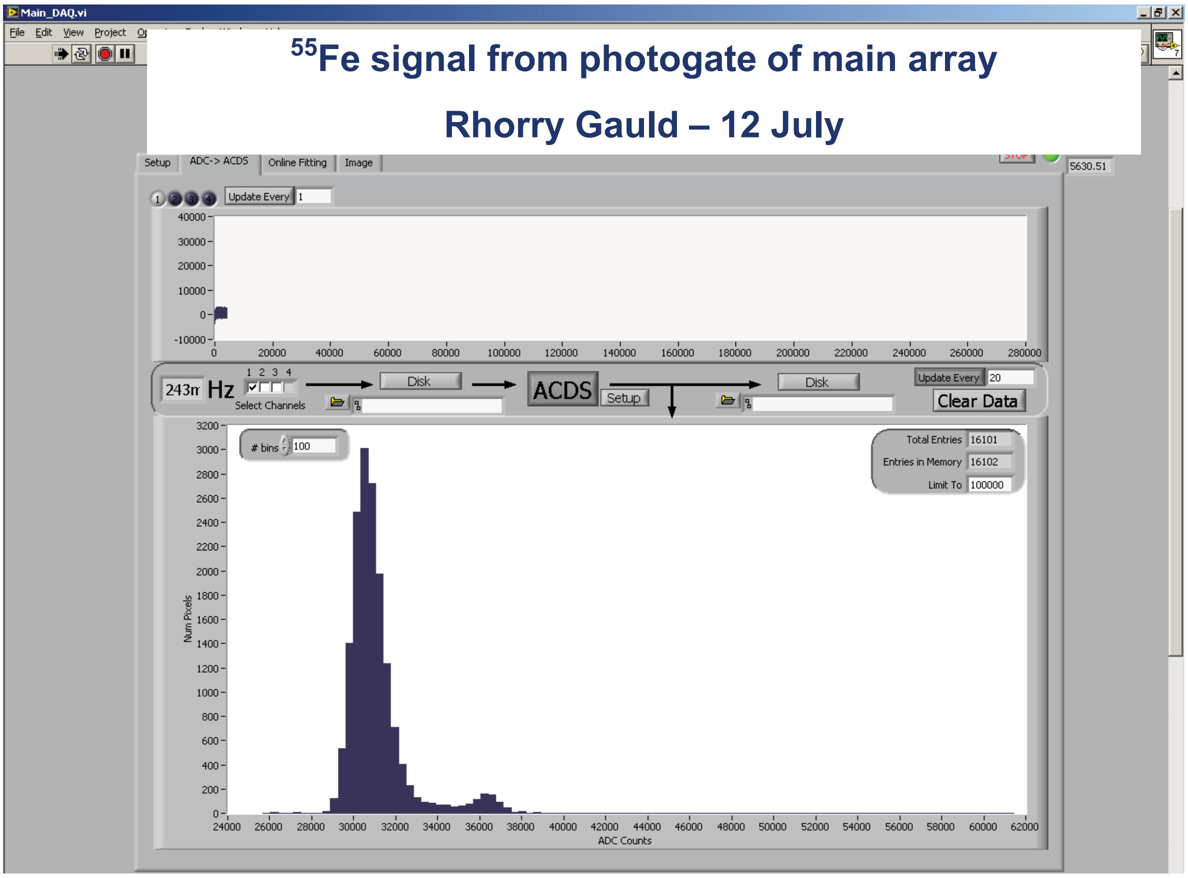
One of 32 readout columns

photogates

Successful charge transfers observed 21st July 2009

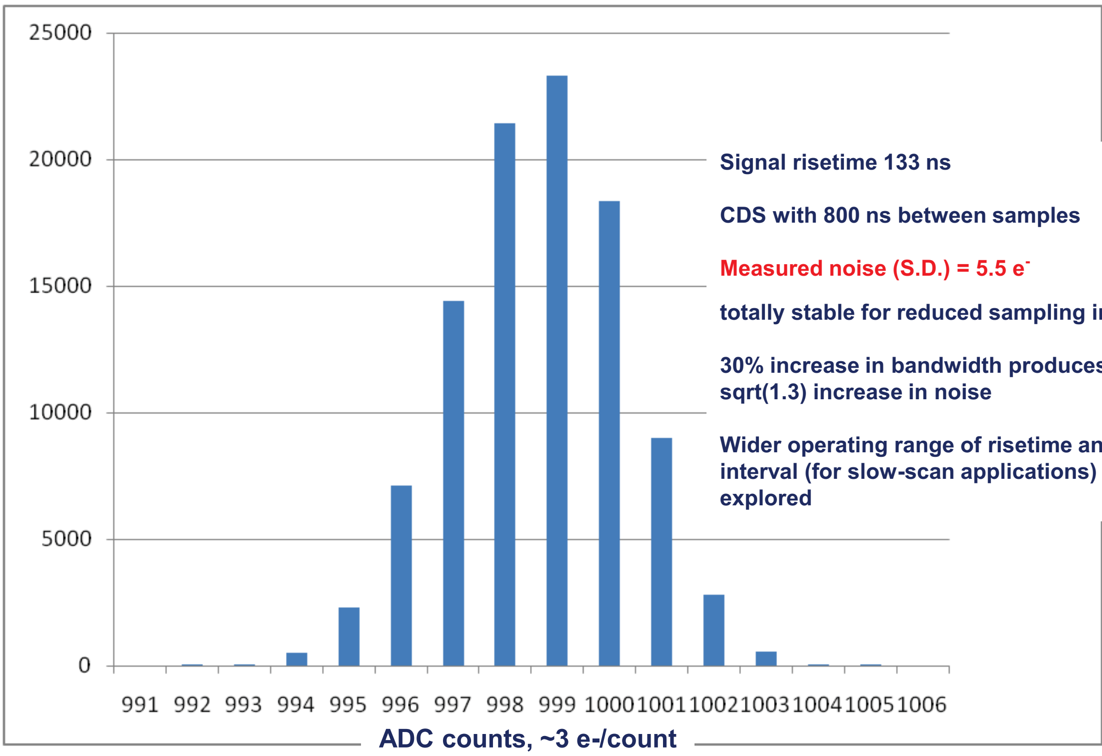
^{55}Fe signal from photogate of main array

Rhorry Gauld – 12 July



- **Signal survives transfer through 20 storage cells!**
- **Broadened by large dark current contribution – as ‘expected’?**
- **Watch this space …**

Noise performance – 2 June 2009 – Gary Zhang – 5.5 e$^-$!



Signal risetime 133 ns

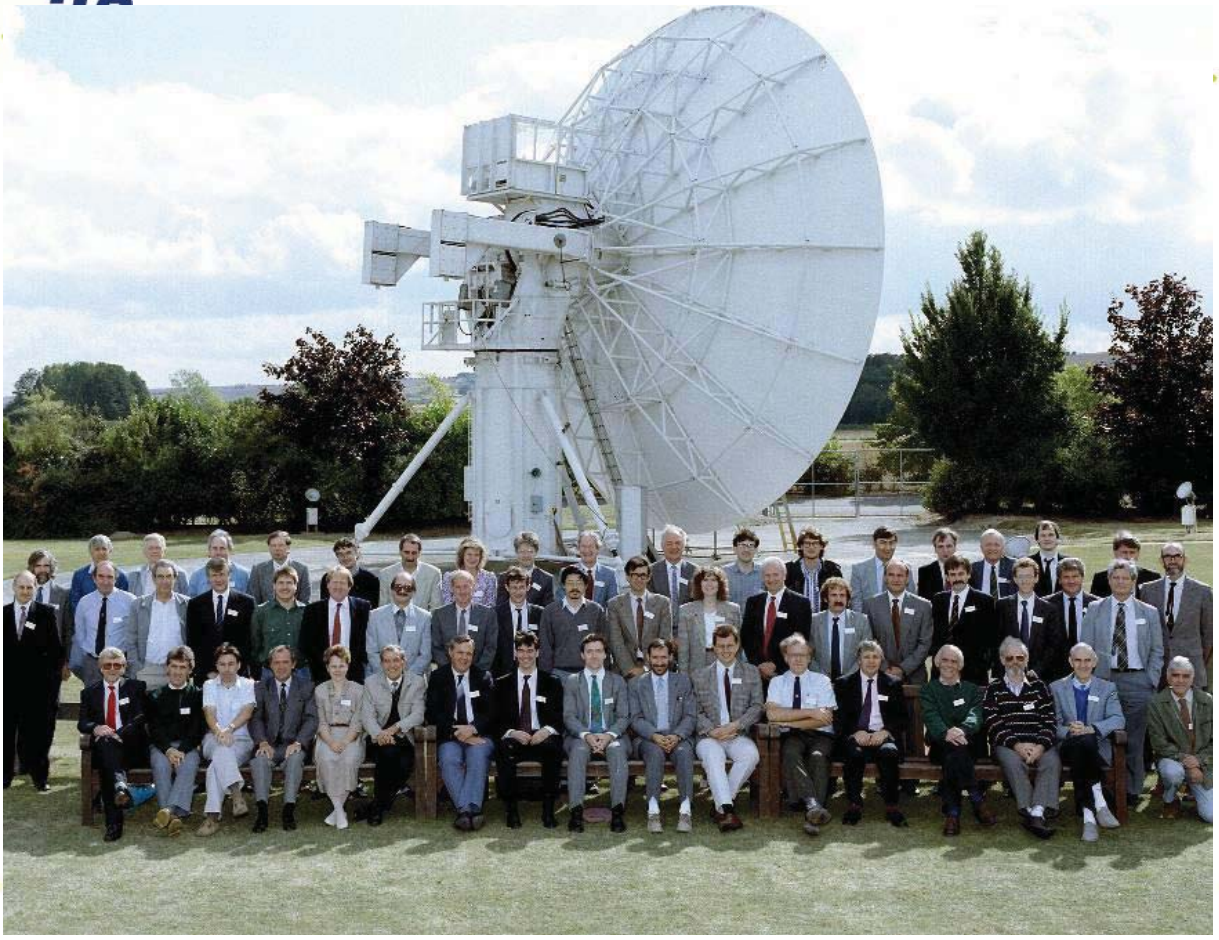
CDS with 800 ns between samples

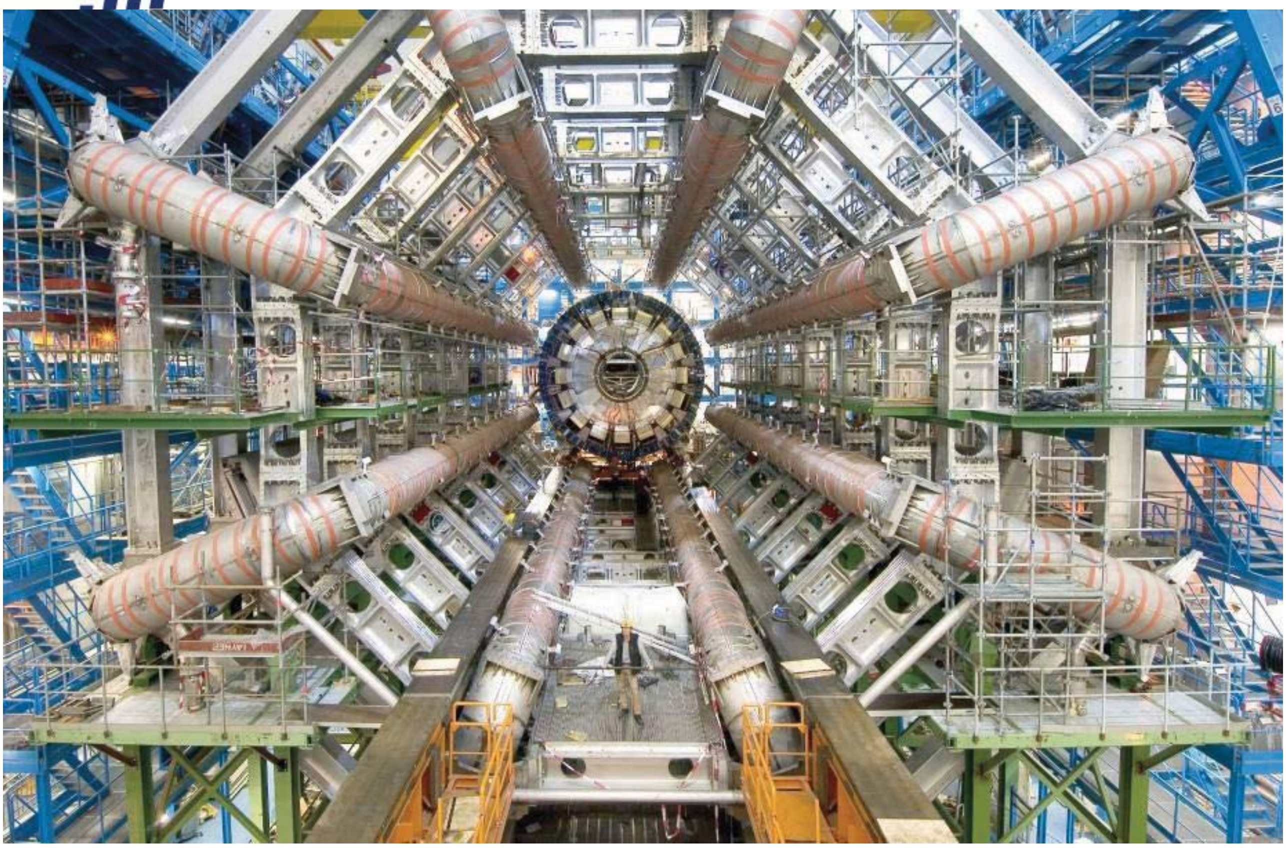
Measured noise (S.D.) = 5.5 e$^-$

totally stable for reduced sampling interval

30% increase in bandwidth produces expected sqrt(1.3) increase in noise

Wider operating range of risetime and CDS interval (for slow-scan applications) will be explored





- Since SLD, there has been an explosion in R&D for all sorts of novel pixel sensors that might be used as vertex detectors at ILC. All are monolithic silicon-based
- For ILC vertex detector, technology choice is wide open between ~ 8 options
- For ILC tracking, there's a suggestion for a Silicon Pixel Tracker (SPT) of ~ 40 Gpixels
- This is realistic, given the timescale: see Gerry Luppino's plot

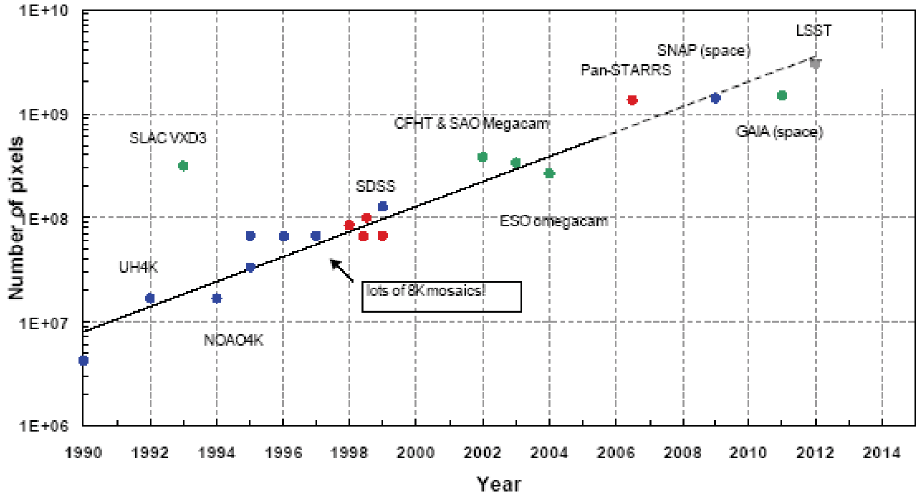


Illustration of focal plane sizes, from Luppino/Burke 'Moores' law

Focal plane size doubles every 2.5 years

From: Burke, Jorden, Vu, SDW Taormina 2005

ILC Detector R&D

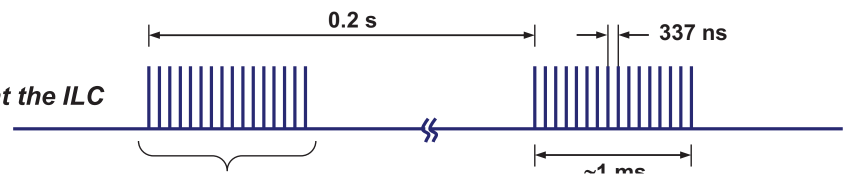
as seen by the Detector R&D Panel 2005-2007 plus updates

Jean-Claude Brient, Chris Damerell, Ray Frey, Dean Karlen, Wolfgang Lohmann, Hwanbae Park, Yasuhiro Sugimoto, Tohru Takeshita, Harry Weerts

Chris Damerell (RAL)

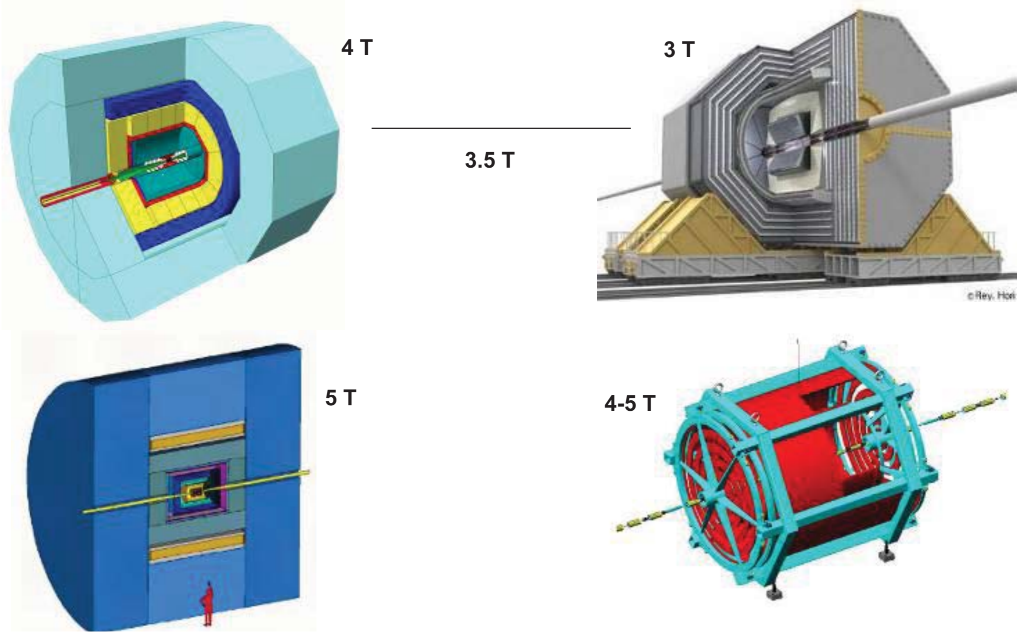
Timely discussion, since the SiD and presumably ILD have been validated, but not the 4th. How to avoid throwing out the baby with the bathwater, if it isn't already too late? Those very talented world experts are being actively wooed for another project. The ILC isn't so strong that it can afford to do this sort of thing (my opinion).

Bunch structure at the ILC



- **Detector options:**
  - Single bunch timing (300 ns for ILC, 0.5 ns for CLIC)
  - Time-slicing of train (eg at 50 μs intervals, 20 slices)
  - Integrate signals through train, with relaxed readout during the inter-train period
- **No 'right answer', despite statement of one collaboration that they will 'time-stamp everything'**
- **There's a power advantage in partial or complete time integration – fine sensor granularity can compensate for pileup from multiple bunch crossings**
- **Lower power enables reduced material budget – extremely desirable for physics with vertexing and tracking systems**
- **There's been a successful history of exploiting granularity/time resolution tradeoffs in ACCMOR and SLD physics programmes**
- **Contrast LHC, where single bunch timing is mandatory**

The three detector concepts



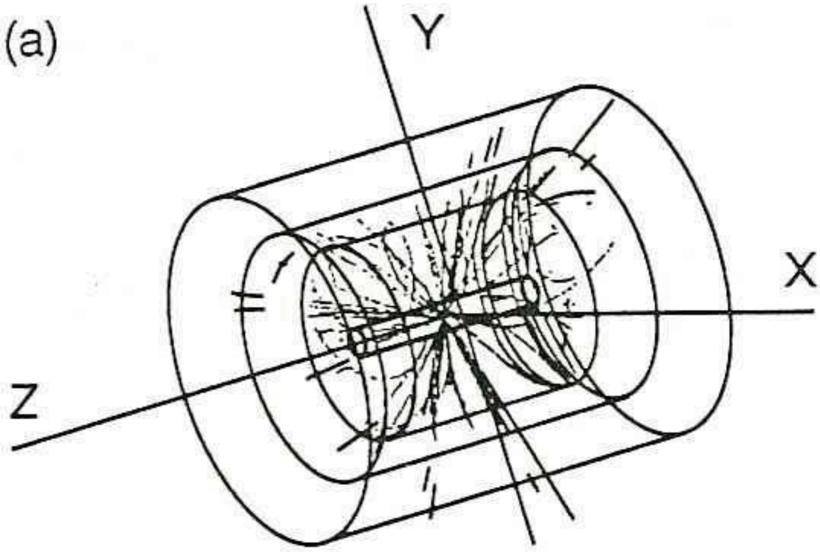
- LDC and GLD have merged into ILD for the LOI and EDR phase
- LOIs if ‘validated’ by the IDAG will progress to ‘light’ or ‘demonstrator’ or ‘practice’ EDRs in 2010 (or 2012?)
- *Detectors to be actually built depend on R&D that should continue till the latest possible time (cf ATLAS and CMS). True or false? ….*

Do we need R&D for ILC detectors?

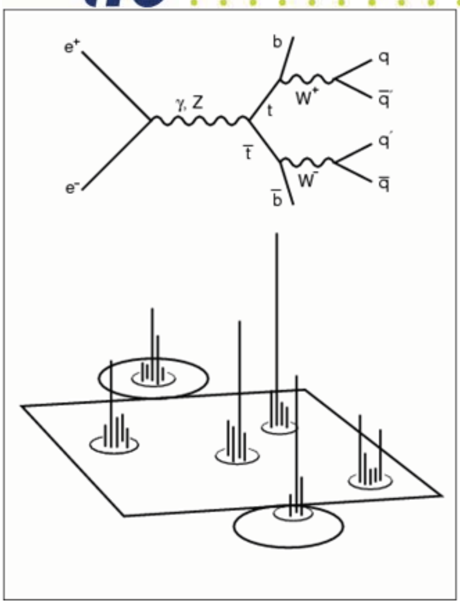
- “After all the R&D for LHC detectors (operating in a more hostile environment), this should be more than enough”
- WRONG!
- To satisfy the very challenging ILC physics goals, we need detectors that nobody knows how to build
- *What is easy, relative to LHC:*
  - Instantaneous particle fluxes
  - Required radiation tolerance

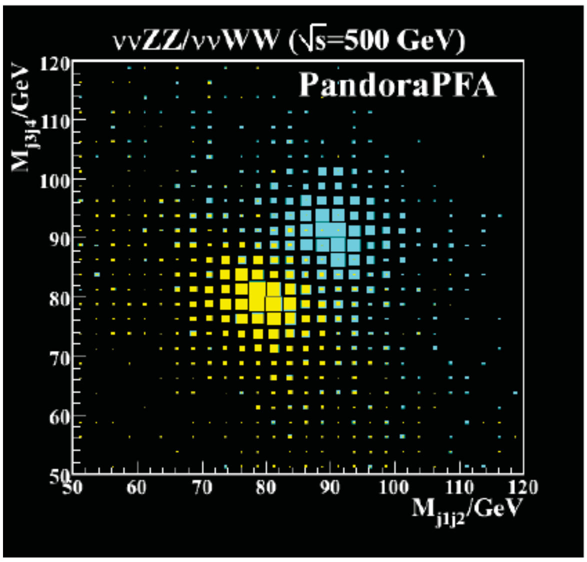
  } $1/R^2$ to inferno at LHC collision point
- *What is difficult, relative to LHC:*
  - The need for extraordinary jet energy resolution and vertexing performance
- *Special opportunities, relative to LHC:*
  - Annihilation of point-like electrons and positrons allows us to observe complex physics processes almost at the Feynman diagram level (very different from colliding bags of quarks and gluons)

$e^+ e^- \rightarrow$ t tbar at 0.5 TeV



At first sight, a confusing spray of particles …





Mark Thompson

The miracle of PFA (or equivalent jet energy resolution) reveals the flow of energy from the quarks of the primary interaction

However, this is still not enough information for full physics analysis ..

Need to tag the heavy flavour (b and c) jets, and for some physics to distinguish between the quark and anti-quark jet

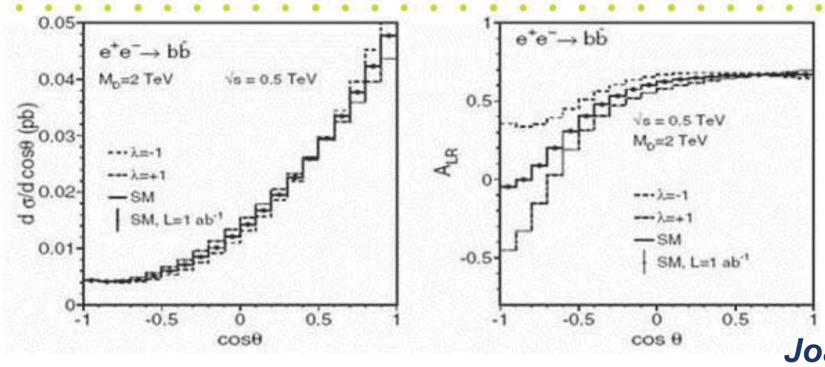
ILC vs LHC vertex detector parameters

Parameter	LHC	ILC	ILC/LHC performance
Sensitive time window	25 ns	~50 μs	~10^{-3}
Radiation resistance	~20 Mrads	~100 krad	~10^{-2}
Tracking precision	~45 μm	~3 μm	15
Layer thickness	2 % X_0	0.1% X_0	20

Which is better – a Sherman tank or a Ferrari?

Each has its uses …

A physics example – $e^+ e^- \rightarrow$ b bbar



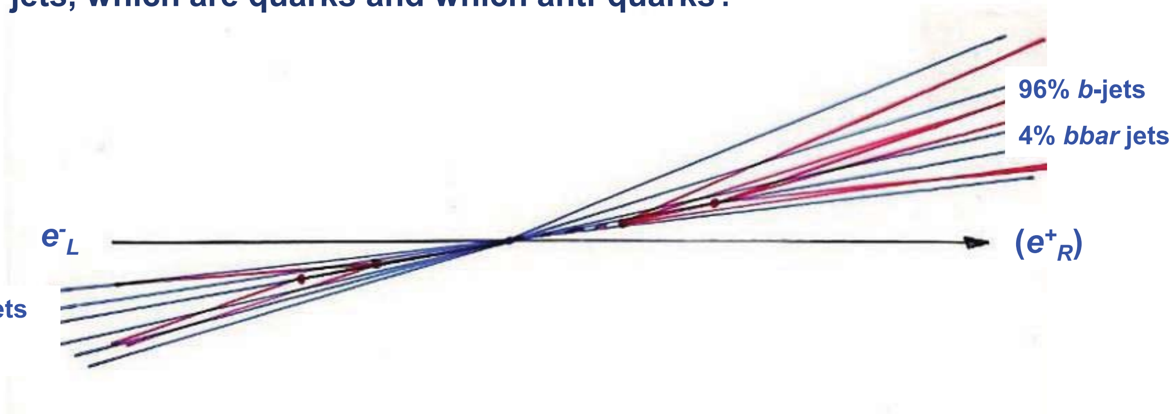
Joanne Hewett, Sabine Riemann

- Need highly polarised electron beams (longitudinal polarisation)
- Need clean b-tag to distinguish from other q-qbar processes
- Need *vertex charge* to distinguish between b and bbar jets, otherwise see folded distns
- These capabilities were pioneered at SLC/SLD, and are unique to the LC technology
- Reward will be sensitivity to new physics via 'oblique corrections', where direct observation is beyond the reach of both ILC and LHC (example of large EDs, with 2TeV scale parameter)
- Another important example – if LHC finds the Higgs, is it the SM Higgs, SUSY Higgs, or what? Precision measurements of branching ratios by ILC will be needed. BR for H $\rightarrow$ c cbar may be decisive, and it's not accessible at LHC

Quark charge determination from 'vertex charge'

e^+e^- -> b bbar from e^+e^- -> q qbar sample by flavour tag based on vertex topology (SLD procedure)

For the b jets, which are quarks and which anti-quarks?



In this event, total charge in decay chain for the backward jet resolves the forward-backward ambiguity – procedure pioneered in, and unique to, SLD *(much cleaner than measurement of 'jet charge')*

Reviews of ILC Detector R&D

PURPOSE:

- **Improved communication leading to enhanced R&D programmes**
- **Get representatives of all R&D groups together for face-to-face discussions**
- **Engage world-leading consultants from outside the ILC community, who would surely provide new insights – *they did!***
- **Ideally, the committee report would do little more than document *mutually agreed* changes from each review *"If you don't have buy-in, you can't effect change."***
- **The reality proved a bit more complicated, but also more productive, due mainly to fresh contributions from those consultants**

SCHEDULE:

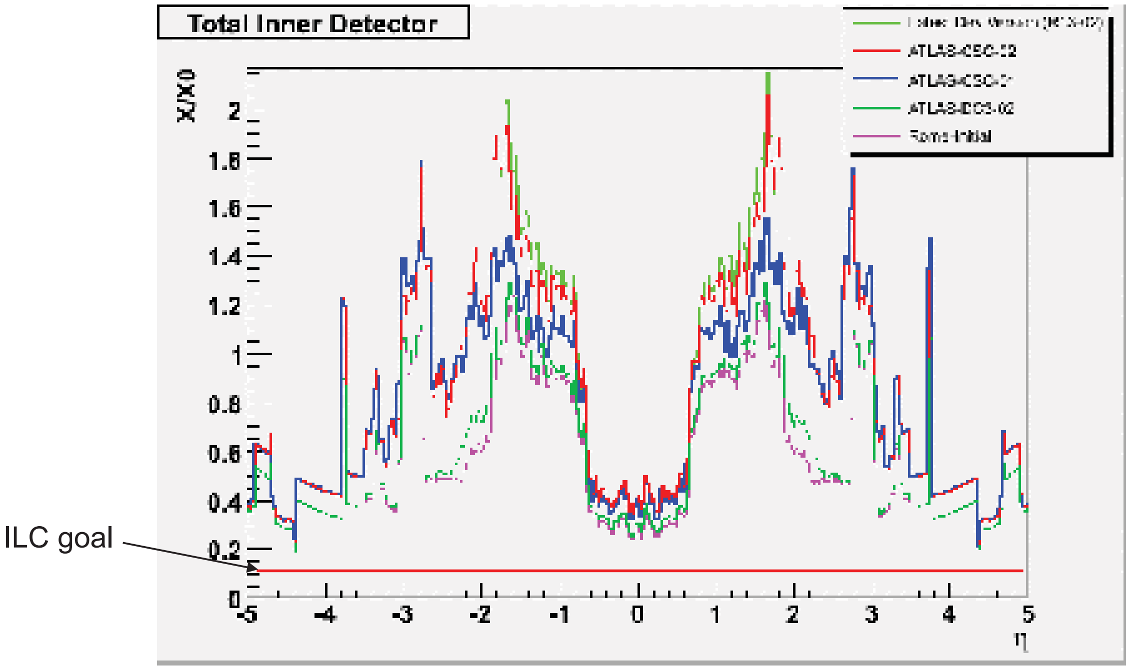
- **3-day reviews were included in the 2007 regional workshops:**
  - **Beijing (Feb '07) Tracking**
  - **DESY (LCWS June '07) Calorimetry**
  - **Fermilab (Oct '07) Vertexing**

Tracking Review Committee

- Panel members: Chris Damerell (chair), Dean Karlen, Wolfgang Lohmann, Hwanbae Park, Harry Weerts
- External consultants: Peter Braun-Munzinger, Ioanis Giomataris, Hideki Hamagaki, Hartmut Sadrozinski, Fabio Sauli, Helmuth Spieler, Mike Tyndel, Yoshinobu Unno
- Regional representatives: Jim Brau, Junji Haba, Bing Zhou
- RDB chair: Bill Willis
- Local tracking experts: Chen Yuanbo, Ouyang Chun
- Admin support: Naomi Nagahashi, Maura Barone, Maxine Hronek, Xu Tongzhou

- We reviewed the LCTPC, CLUCOU, SiLC and SiD tracking R&D collaborations
- We were extremely impressed by the R&D programmes of all these groups, in some cases with very limited resources
- However, we concluded that we are currently far from the goals, for all tracking options
- Building a tracking system with excellent performance for θ_p >7 degrees will be challenging. *Never achieved before and feasibility is not yet demonstrated*
- Forward tracking has generally performed badly. We all know the solution (drastic reduction in material budget) but *can this be achieved in practice?*
- We became convinced of the need to construct large prototypes (~1 m diameter), and operate them under ILC-like beam conditions in a 3-5 T field, to establish what performance will be achievable at ILC, both for central and forward tracking
- Not all the R&D collaborations felt that this would be necessary

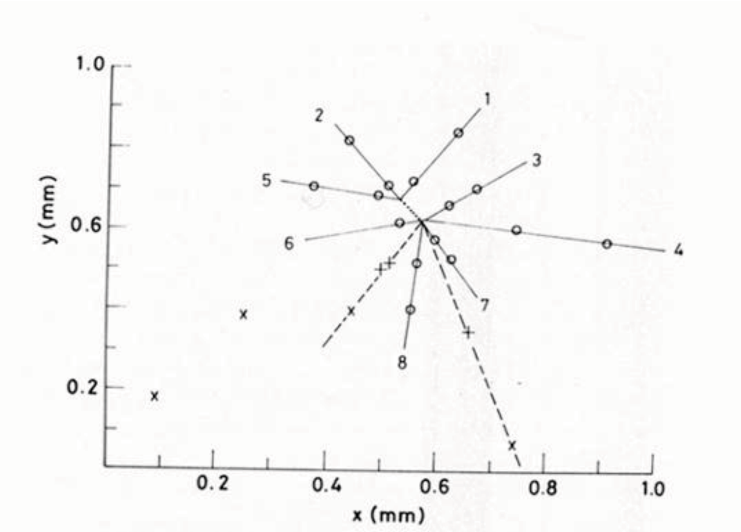
Lessons from LHC (ATLAS)

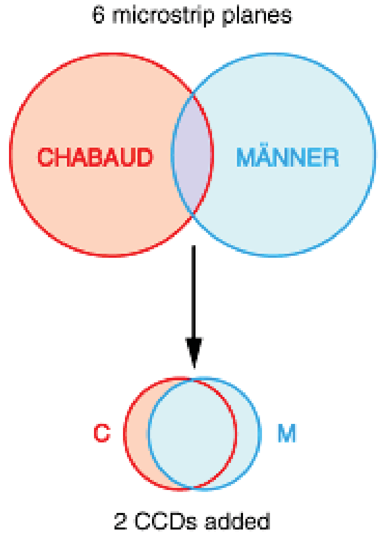


A new idea – Silicon Pixel Tracker

- **The most serious concern of the committee was the material budget, particularly how badly this might degrade the forward tracking:**
  - **For TPC tracker, can the endplate thickness really be reduced to 'well below 0.3 X_0 possibly 0.1 X_0'? Our expert consultants were extremely doubtful**
  - **Franco Grancagnolo's drift chamber could probably be made pretty thin, but would it provide robust track finding for high energy jets? Detailed simulations since done – now looks quite convincing. But one still has to decide about the forward tracking**
  - **For a silicon strip tracker, everyone now agrees that the 'momenter' concept is flawed. Will 5 single-sided layers (barrel or disks) suffice, or will there be serious pattern recognition problems, for example for high energy jets containing long-lived Bs, necessitating more layers and hence more material?**
- **Discussions with our consultants led to a new suggestion – a silicon pixel tracker (SPT) which could deliver excellent pattern recognition for tracks in high energy jets, with very little material over the full range of polar angles**

- A pixel tracker provides far more information per layer, is entirely free of ghost hits, and has a proven record for excellent pattern recognition compared to microstrips in high multiplicity jet-like events (ACCMOR Collaboration, mid-1980s)

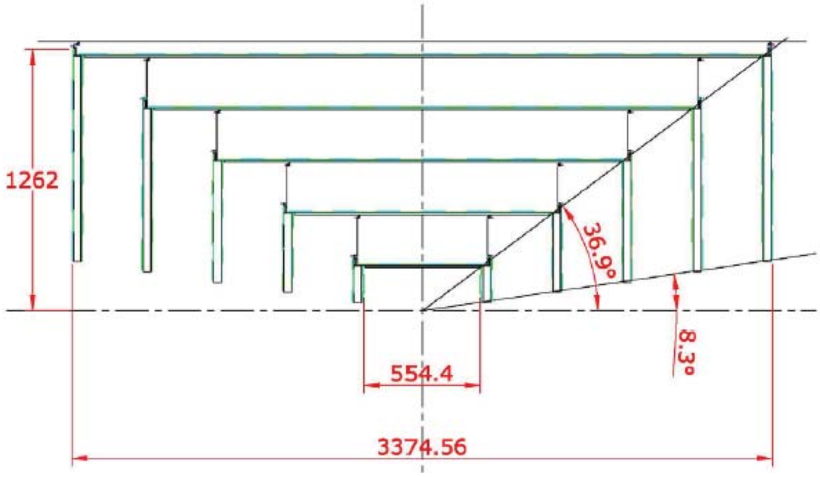




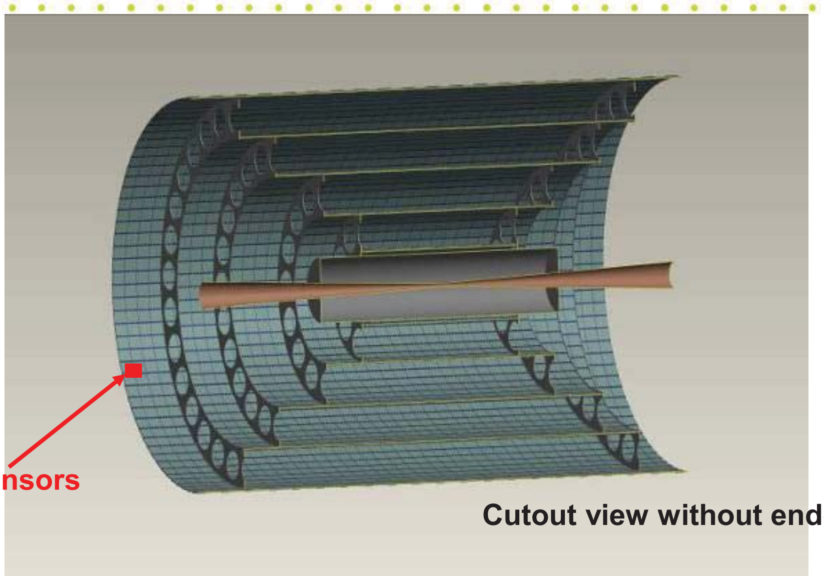
200 GeV 'jets', Clean pattern recognition by two pixel planes 1 and 2 cm beyond the IP

- A tracker made with *monolithic pixel sensors* could provide the thinnest layers (~50 μm Si plus support structure) and the maximum information per layer, hence require the smallest number of layers
- If 5 layers of microstrips is marginal for SiD, it would be *overkill* if they switched to a SPT, and each layer could be thinner
- At first sight, it could be a challenge to make such a detector with sufficiently low power to preserve gas cooling
- This can be achieved by *dispensing with single-bunch time stamping* and even time slicing over most of the angular coverage, relying on the ECAL to label each track with its bunch number in the train
- Remember that all measurable tracks end up in the ECAL, including curlers [tracks with p_T < ~ 0.5 GeV/c, seen only in the vertex detector, are a special case]

SiD tracker layout
(silicon microstrips)



- 5 barrels and 4 endcaps, total area = 70 m^2
- Everyone (?) now accepts need for standalone trk finding in this subsystem
- With 50 μm square pixels – 28 Gpix system
- Low mass support, gas cooling
- If each sensor is 8 cm × 8 cm (2.6 Mpix): 11,000 sensors is total
- Note: forward disks will need time stamping, due to high 2-photon bgd (study by Marcel Vos)
- See Sunday's talk for a promising technology, within the family of charge-coupled CMOS pixel devices



one of 11,000 sensors
8x8 cm^2

Cutout view without endcaps

- SiC foam support ladders, linked mechanically to one another along their length
- 5 closed cylinders (incl endcaps, not shown) will have excellent mechanical stability
- ~0.6% X_0 per layer, 3.0% X_0 total, over full polar angle range, plus <1% X_0 from VXD system (goal)
- Scale is in line with trends in astronomical wide-field focal plane systems by 2020

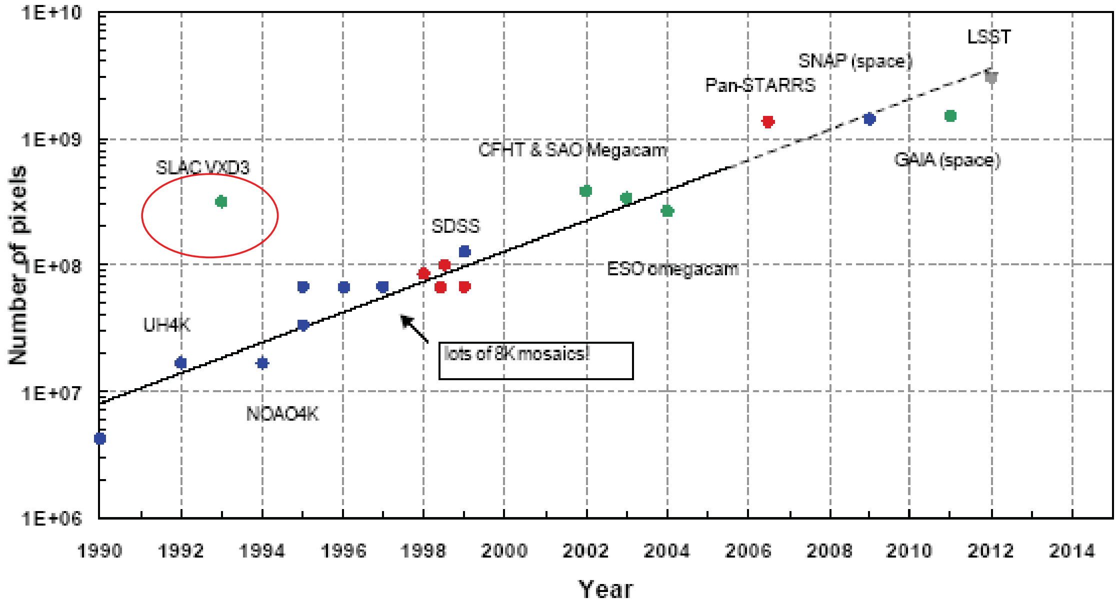


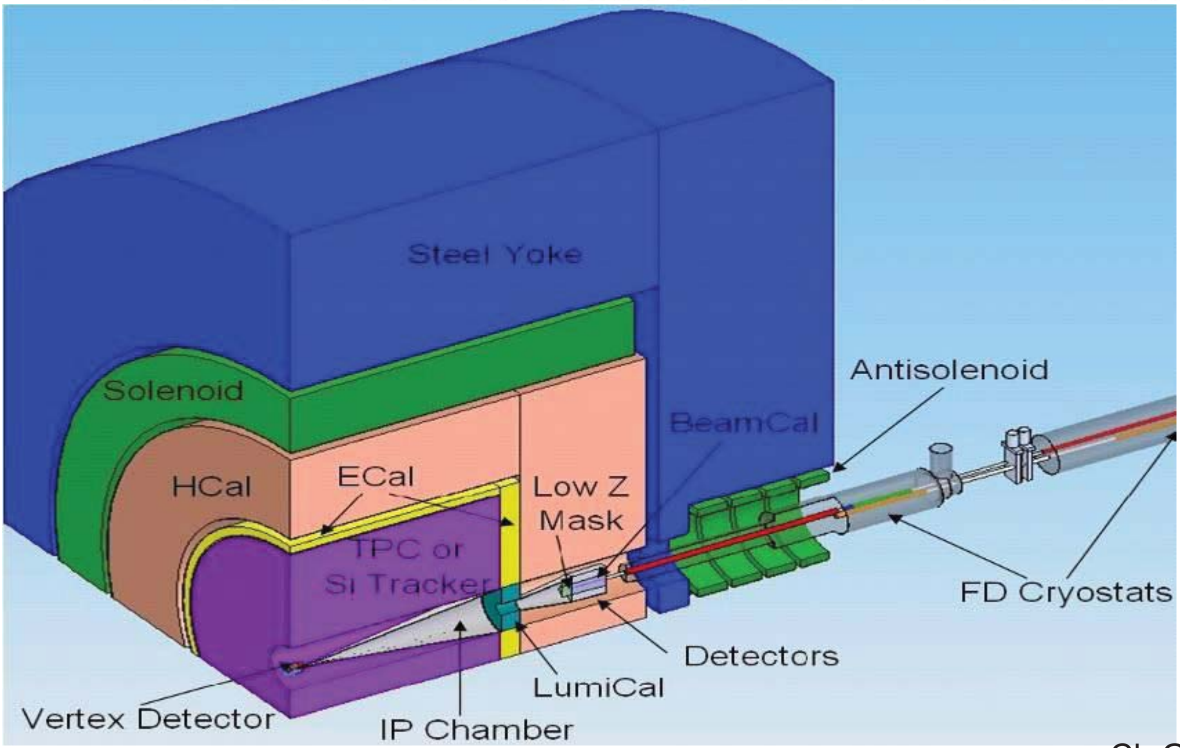
Illustration of focal plane sizes, from Luppino/Burke 'Moores' law

Focal plane size doubles every 2.5 years

From: Burke, Jorden, Vu, SDW Taormina 2005

Calorimetry Review Committee

- **Panel members: Jean-Claude Brient, Chris Damerell, Wolfgang Lohmann (chair), Ray Frey**
- **External consultants: Marcella Diemoz, Andrey Golutvin, Kazuhiko Hara, Robert Klanner, Peter Loch, Pierre Petroff, Jm Pilcher, Daniel Pitzl, Peter Schacht, Chris Tully**
- **Regional representatives: Junji Haba, Michael Rijssenbeek, Jan Timmermans**
- **RDB chair: Bill Willis**
- **Admin support: Martina Mende, Naomi Nagahashi**

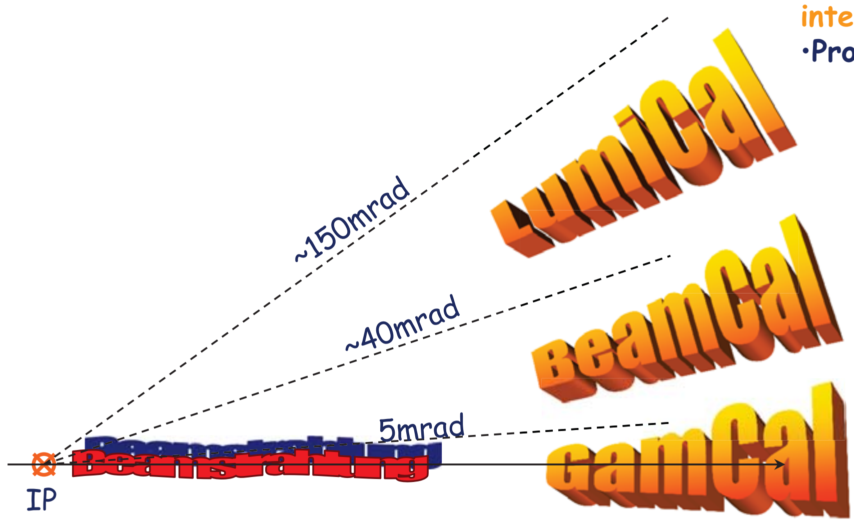


Ch Grah

Overview of the review

- **Two main categories:**
  - **Very forward calorimetry (precision luminosity, hermeticity, beam diagnosics)**
    - **FCAL Collaboration (15 groups)**
  - **Doing a great job, but need additional resources, specially in USA**
  - **General calorimetry (precise jet energy measurement in multi-jet events, ΔE = 30%sqrt(E)**
    - **PFA approach: CALICE collab (41 gps), SiDCAL collab (17 gps, some in CALICE)**
    - **Compensating calorimetry: DREAM collab (8 gps), Fermilab gp**
  - **We were not able to exclude either option: much more work is required (and we might eventually need *both* to do the physics: PFA in barrel and compensating calorimetry forward)**

Tasks of the Forward Region



•Precise measurement of the integrated luminosity ($\Delta L/L \sim 10^{-4}$)
•Provide 2-photon veto

•Provide 2-photon veto
•Serve the beamdiagnostics using beamstrahlung pairs

•Serve the beamdiagnostics using beamstrahlung photons

Ch Grah

Challenges:
High precision, high occupancy, high radiation dose, fast read-out!

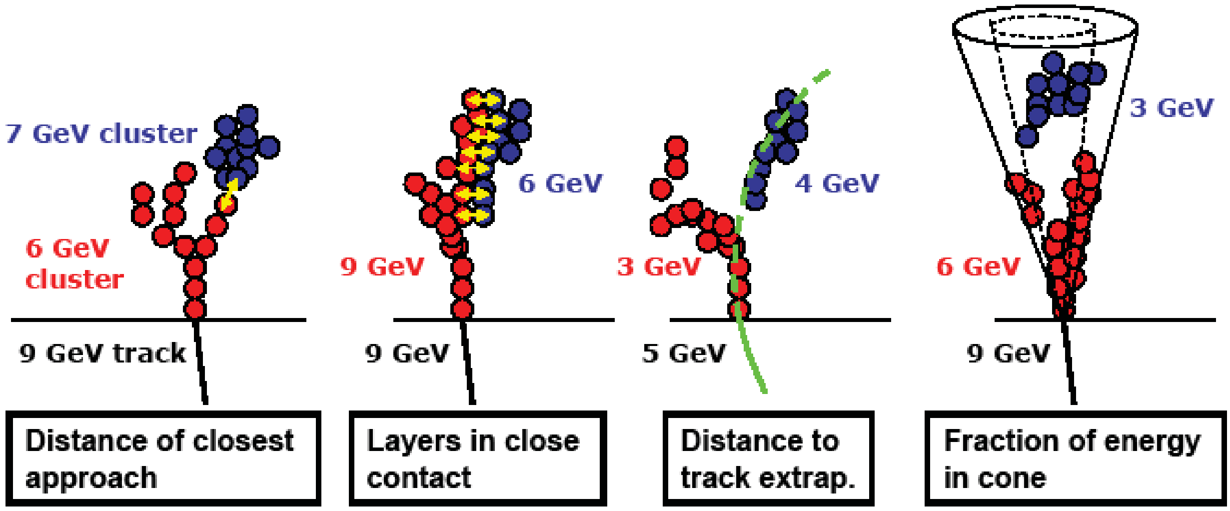
Main technical recommendations (FCAL)

- **Impressive report – physics requirements and technical implications were clearly presented**
- **Design of LumiCal and BeamCal well advanced – GamCal (BS monitor) studies are at an early stage**
- **BeamCal sensor development profits from close collaboration with groups developing rad hard sensors for hadron machines, notably sLHC**
- **Need increased funding for travel, for their dedicated US collaborators (even before FY08 disaster), and for system-level engineering**

PFA approach to jet energy measurement

- Goal is to separate depositions from charged and neutral hadrons in the ECAL/HCAL system. This is particularly challenging in the core of jets
- Challenge *('confusion term')* increases with jet energy and with reduced polar angle

★ Look for "evidence" that a cluster is associated with another

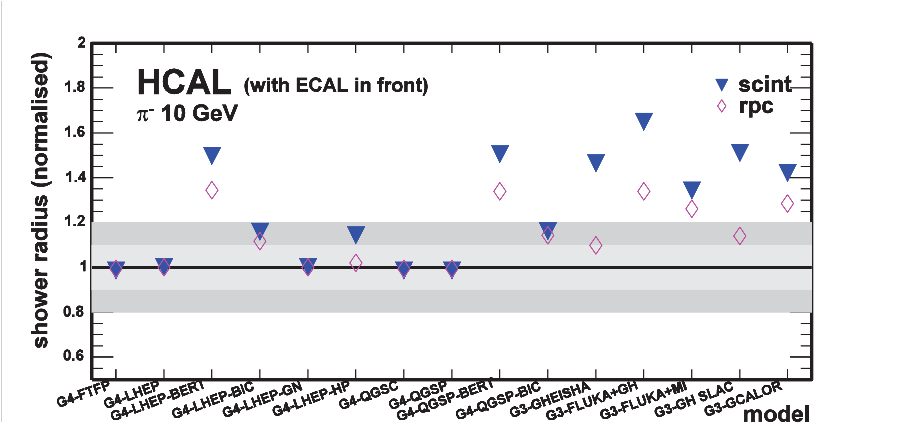


Mark Thomson

- Impressive results based entirely on *simulations*. Can such performance be achieved in a real system?
- If possible, obtain data from charged and neutral hadrons in 'physics prototype' calorimeter system, and use them in conjunction with simulation of ILC jets to create more realistic hit patterns in the calorimetry system, hence determine how well PFA will handle real ILC events (not quite a 'shower library, but …)
- There has been progress since our review (Jose Repond, Rajendran Raja) in establishing practical conditions for calibration with tagged neutrals (neutrons, K_L, even anti-neutrons) using the MIPP2 facility in MCentre at Fermilab. DAQ problems of concern previously can be overcome
- However, in view of Fermilab backpeddling on almost anything to do with ILC, this may be shelved
- This programme requires a significant effort, but this is better than discovering in 2025 that the PFA approach was a poor second choice
- The vertex detector and tracking systems can and probably will be upgraded during ILC running, but not the coil or calorimetry – we do need to get these right when experiments choose their technologies

Main recommendations (PFA systems)

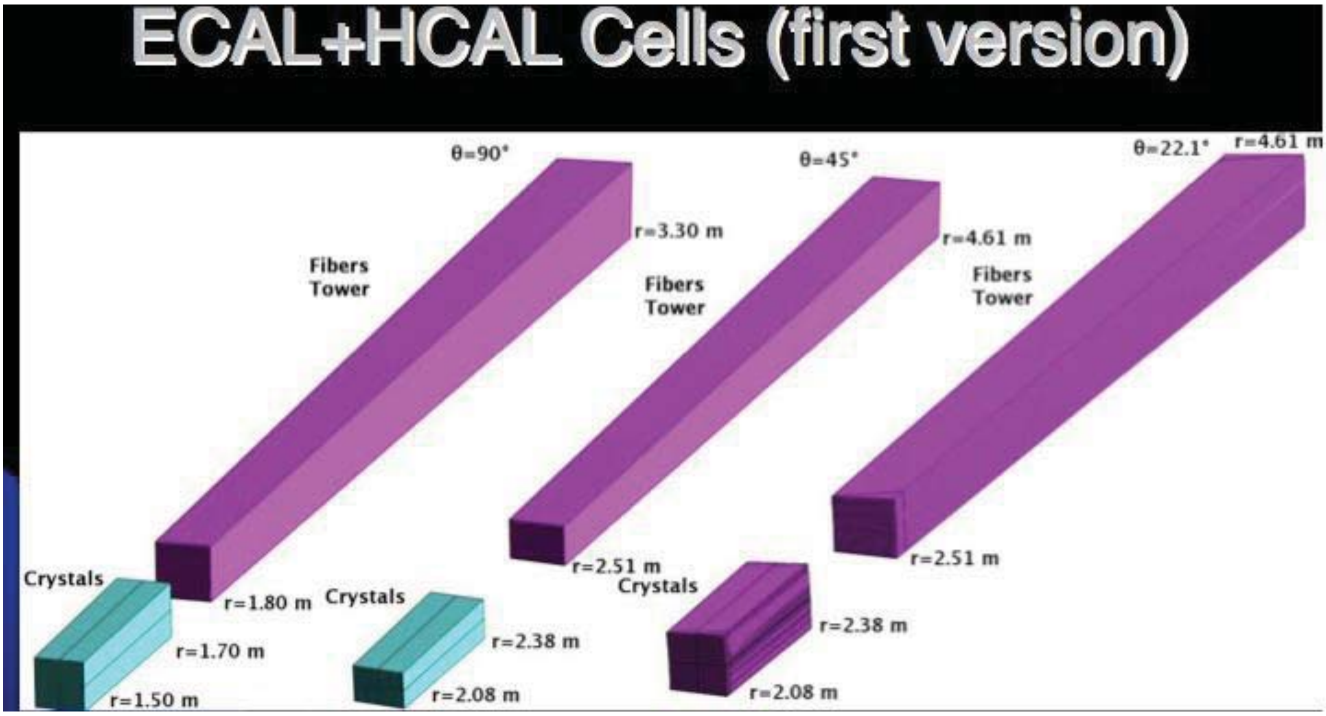
- While extremely promising, all studies to date (beyond the early experience with ALEPH and SLD) are based on *simulations,* hence subject to considerable uncertainty



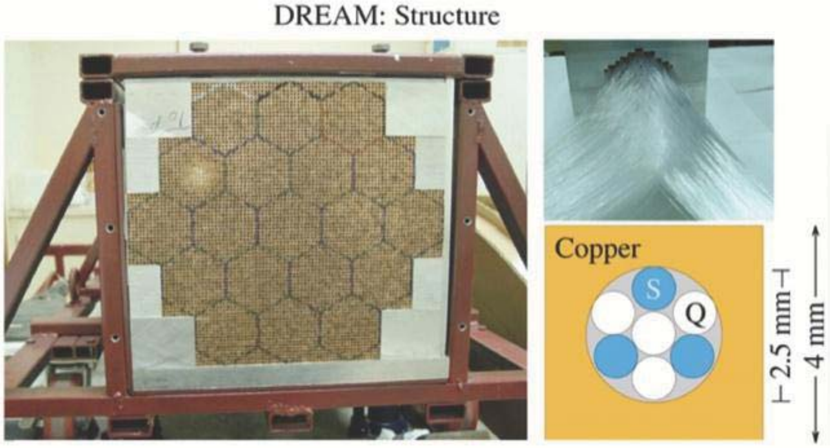
- These are only the *average* shower radii. There is much greater uncertainty in the shape variability between individual showers, involving different inelastic scattering processes

- Simulations alone cannot be trusted. Given the need to disentangle hits from charged and neutral showers, data are desirable on both, in large-scale 'physics prototypes' to:
  - Establish the performance truly achievable with such a calorimetry system
  - Establish which HCAL sensor technology (scintillator, RPCs, etc) will give the best performance. There is also (within CALICE) the option of a digital ECAL …)

Compensating calorimetry option



Promising test beam results



- Make no attempt to resolve the particles in jet cores, within the calorimeter

- Crystal EM section, with dual readout of scintillation and Cerenkov light by timing , followed by a hadronic section with dual readout by quartz and scintillator fibres

- No longitudinal segmentation, but SiPMs and local readout chips will permit excellent hermeticity. HCAL thickness can be 10λ or more

- Simulations indicate they could achieve ΔE = 20-25%sqrt(E) for isolated jets. Not clear yet how well their *pfa* (John Hauptman) will sort out the crosstalk in multi-jet events

Main recommendations (compensating calorimetry)

- PFA performance is expected to degrade in the forward region, where for t-tbar and much BSM physics, one or more jets will generally be directed

- Cannot afford to let the tracking 'go to hell in the forward region' as in the past

- Less spreading of charged tracks may also favour a hardware compensating calorimeter and and *pfa* approach

- Before moving to a large scale prototype, the review recommended they investigate a number of concerns, some by simulations, others by lab tests – now largely accomplished

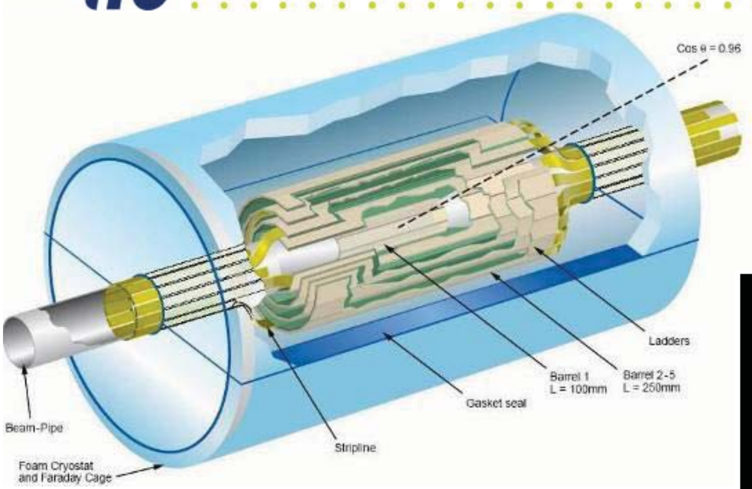
- Their collaboration needs more people, and we encouraged others to join. Their approach could prove to be the outright winner – we simply don't know yet

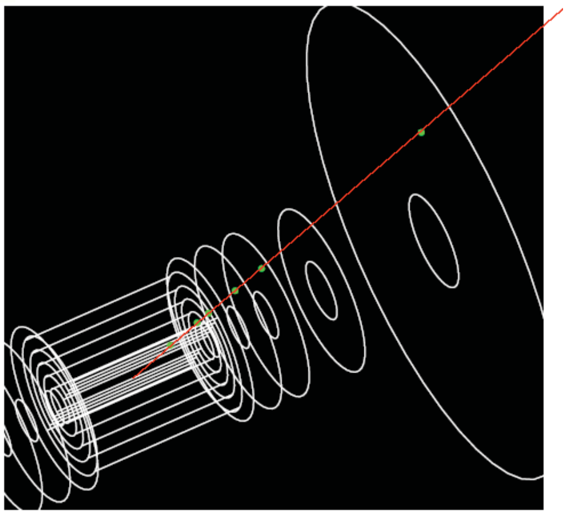
- Some good news! John Hauptman e-mailed me yesterday that they have been funded to build SuperDREAM, have support for their SiPM R&D, and have been joined by a new University group with independent funding

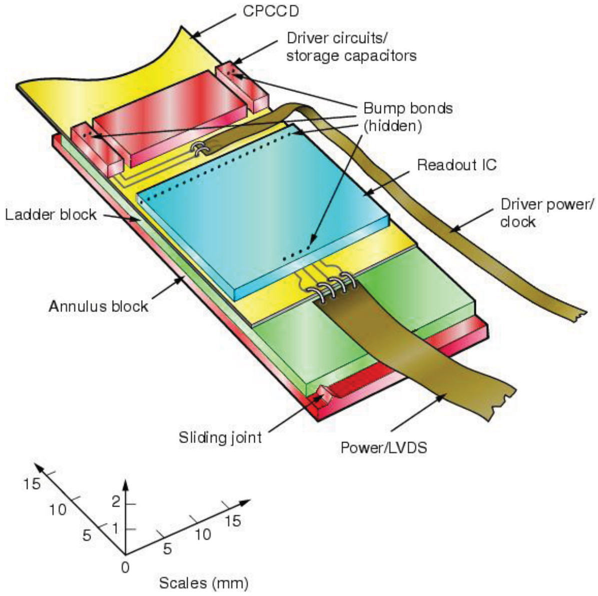
Vertexing Review Committee

- Panel members: Chris Damerell, Hwanbae Park (chair)
- External consultants: Yasuo Arai, Dave Christian, Masashi Hazumi, Gerhard Lutz, Pavel Rehak, Petra Riedler, Steve Watts
- Regional representatives: Tim Bolton, Chris Damerell, (Junji Haba)
- RDB chair: Bill Willis
- Local vertexing experts: Simon Kwan, Lenny Spiegel
- Admin support: Naomi Nagahashi

ILC vertex detector – two main layout options







Optimal geometry will depend on ladder-end details that are not yet defined for *any* technology

VXD technologies

- **All *NINE** approaches aim for ~3 μm precision and <40 μm 2-hit resolution**
- **Target material budget is ~0.1% X_0 per layer**
- **They vary from single-bunch time stamping to time integrating with special compensating features**
- **List them in approximate order of adventurousness – one or two are more likely to be candidates for second generation upgrades**
- ***Now 7 or 8**

FPCCD – Yasuhiro Sugimoto

- CCD with 5 μm pixels, read out once per train; 20 times finer pixel granularity instead of 20 time slices
- Pair bgd rejected by mini-vectors indicating track direction
- Bgd rejection depends on closely spaced pairs of sensors through the barrel
- All signal processing is column parallel at ends of ladder, beyond active area
- Possible showstopper**:
  - real bgd rejection factor proves to be less than ~20 as simulated

** one example showstopper per project, all agreed by the project leaders

CMOS MAPS (MIMOSA) – Marc Winter

- 3T architecture, limited to NMOS transistors in pixel
- Rolling shutter – 'row parallel' to get the required readout rate
- Goal is 25 μs (40 frames) on inner layer. Larger pixels on outer layers. Former may be too conservative, latter may be too optimistic. Detailed simulations needed
- Plan to use 10-20 sensors per ladder, due to yield considerations
- Possible showstopper:
  - Frame-rate CDS, not robust against baseline drift and low fcy pickup

DEEP n-well – Valerio Re

- Full CMOS in pixel, collecting signal charge on the deep n-well that houses the NMOS transistors (triple-well process)
- In-pixel data sparsification and time-stamping with 30 μs precision
- Goal is ~15 μm pixels, so binary readout OK
- CDS achieved by in-pixel time-invariant signal processing
- Possible showstopper:
  - Fall short of full min-I efficiency due to charge collection to competing in-pixel n-wells

CAP – Gary Varner

- CMOS MAPS, with signal storage (after charge-to-voltage conversion) on in-pixel capacitors
- Aim for time slice < 50 μs with >10 storage cells, but difficult to achieve performance with adequate noise performance
- Needs fast shaping time to accept signal from last BX before the sample. Signals are referenced to a baseline established at start of train, so there is exposure to baseline drift
- Possible showstopper:
  - Insufficient pickup immunity due to charge-to-voltage conversion during the noisy bunch train

DEPFET – Laci Andricek

- Signal charge stored on ‘internal gate’ – unique in-house technology
- Complex design – as well as sensors, need steering chips along edge of ladder, and readout chips bump-bonded at ladder ends
- Possible showstopper:
  - Failure to reach required readout rate with full system

Chronopixels – Dave Strom

- Goal is to time-stamp (single bunch) by pixel functionality that can fit into a 10 μm pixel (full CMOS wirh 45 nm design rules)
- Deep p-well to shield the signal charge from the PMOS transistors
- Binary readout will give sufficient precision
- Possible showstopper:
  - Unacceptably high power dissipation

Vertically integrated pixel detectors (SOI & 3D) – Ray Yarema

- An impressive strategy to be liberated from the constraints of CMOS by developing tiered systems
- Potential for data-driven systems with single-bunch time stamping, the 'physicists dream'
- Plan is for very small pixels with binary readout, like the chronopixels
- Problems from back-gate effect with first manufacturers (Lincoln Labs) but a potentially clean solution with Tezzaron (wafer fab by Chartered Semiconductos in Singapore)
- Cu-Cu thermocompression bonding (also being developed by IBM, MIT, …)
- Chartered currently process 1000 wafers/month
- Possible showstopper:
  - 4 Gpixels may exceed the power limits for gas cooling

ISIS – Andrei Nomerotski

- Possible showstoppers:
  - inefficient transfer from photogate to storage register (due to tails on deep p implant etc)
  - poor c.t.e. within storage register (problems of buried channel and/or gaps between poly gates – *potential pockets*)
  - problems scaling down to 20 μm imaging pixel
  - problems stitching for full-scale devices (~12x2 cm^2)

Most of the VXD R&D groups hope to have full-scale ladders in test beams by 2012, as part of the demonstration of technical capability for an ILC facility able to satisfy all the performance goals set by the physics

In the vertex review, Su Dong pointed out that a mixed system, with a higher performance technology for layer-1, might be optimal for ILC

In the meantime, message to funding agencies and LOI collaborations: don't be in a rush to down-select!

SLC Experiments Workshop 1982,
just 8 years before start of SLC

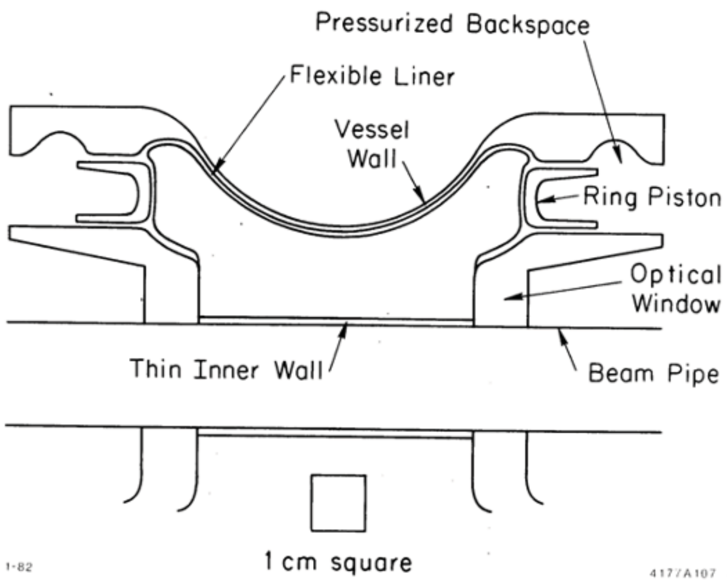
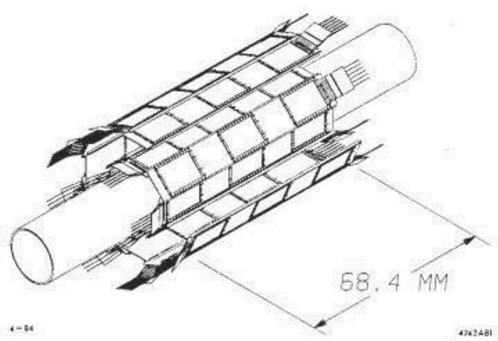
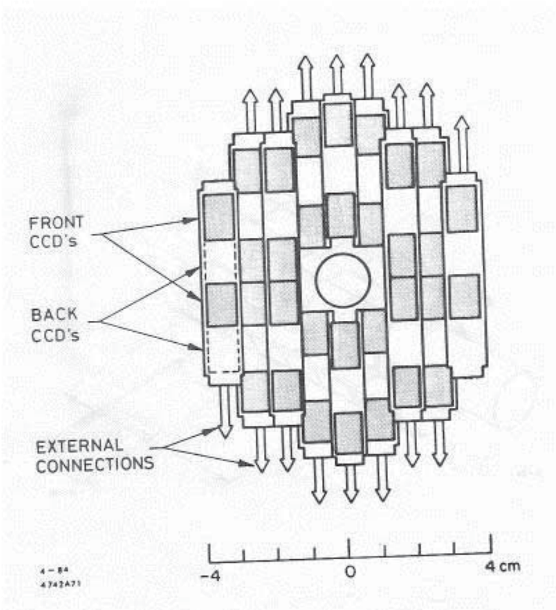


Fig. 7. Conceptual design of a propane bubble chamber vertex detector.

SLD's Vertex Detector Design in 1984
CCDs had demonstrated efficiency for min-I particles
R_{bp} was still 10 mm



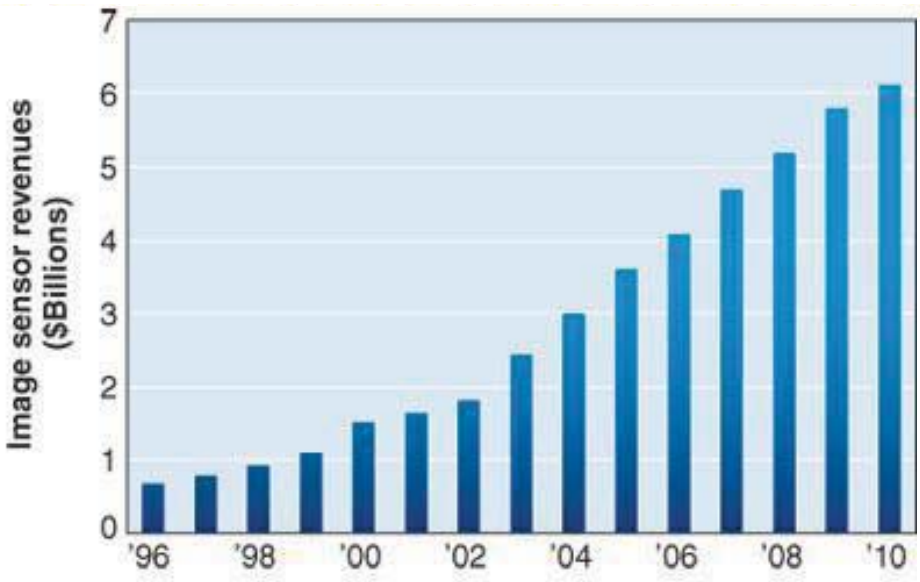


What was installed in 1995:
307 Mpixel CCD system, with
R_{bp} = 25 mm

Conclusions (tracking and vertexing)

- The increasing availability of charge-coupled CMOS pixel structures (large area photodiodes and photogates, 4T structures permitting CDS, and charge storage registers) are opening new windows for vertex detectors and particle tracking systems
- For an ILC tracker, such structures would permit the accumulation of one or more packets of signal charge, integrating or time-slicing the bunch train, followed by readout in which the charge sensing process is decoupled, both in terms of sense node capacitance and in time (allowing leisurely readout in the quiet period between bunch trains) – excellent noise performance
- Logically this is the opposite of 'pulsed power'; the readout is inactive through the noisy bunch train, and proceeds steadily through the inter-train period. Average power is probably easily compatible with gas cooling
- As well as unprecedented vertex detector capability, the requirement of excellent tracking performance, with a detector that is effectively transparent to photons over the full polar angle range, can possibly be realised by this approach
- Maybe 3% of the tracker (fwd disks) will need time stamping, the break point to be determined by simulations

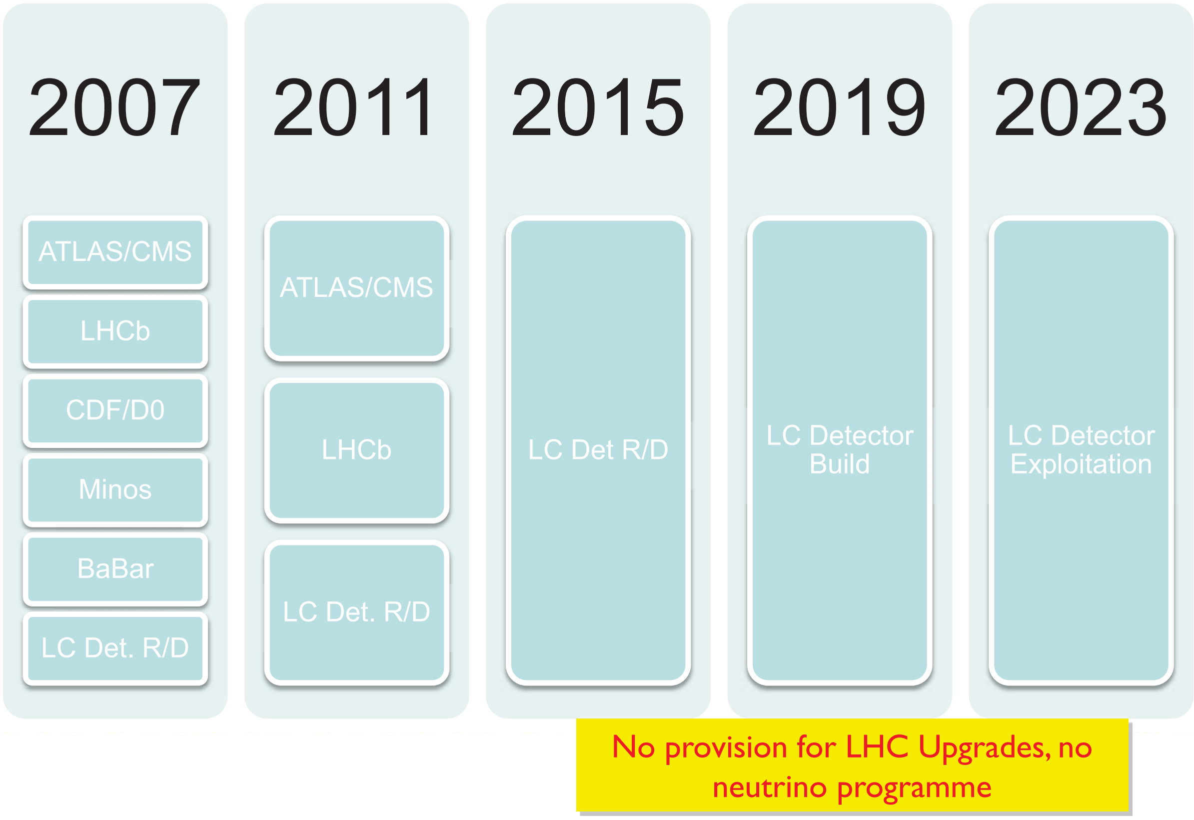
Additional Material

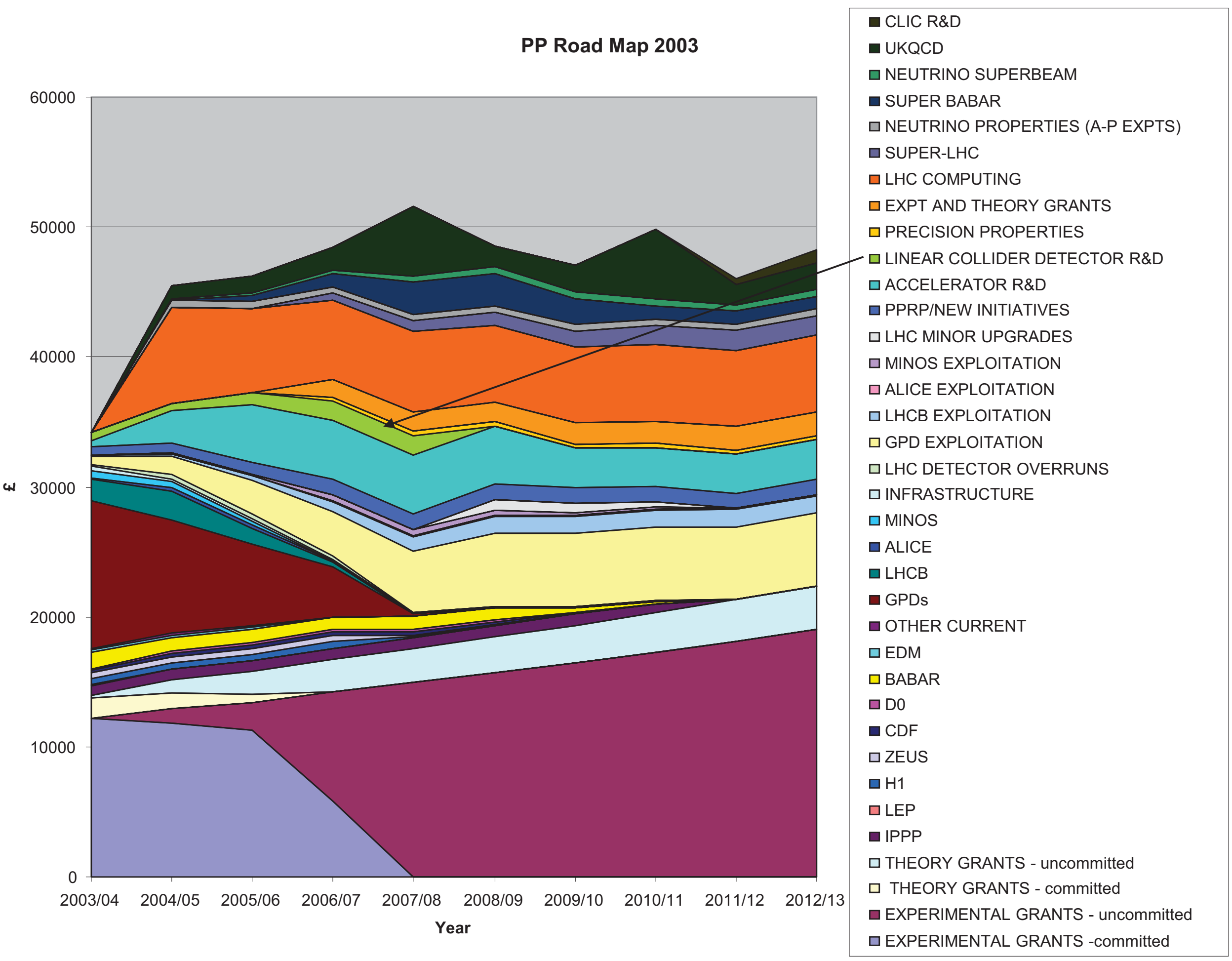


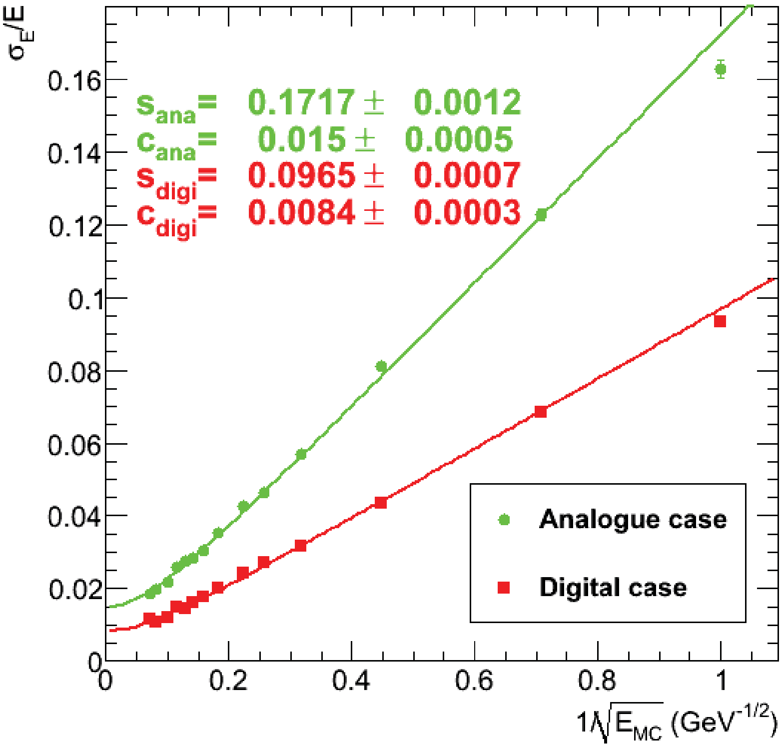
As with developments in microelectronics, we (the particle physics community) are now small fish in a very large pond.

Jordan Nash, Town Meeting, April 1, 2008

What was in the planning tables coming into PR

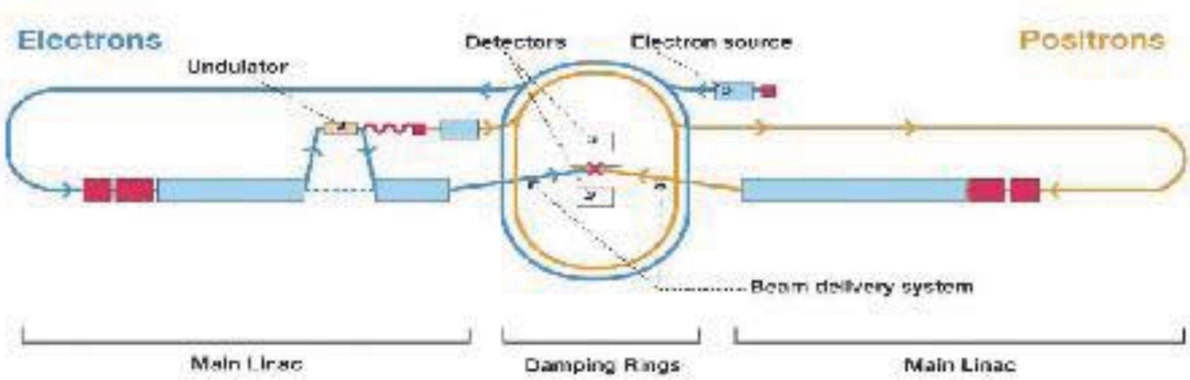






σ_E/E
s_{ana}= 0.1717 ± 0.0012
c_{ana}= 0.015 ± 0.0005
s_{digi}= 0.0965 ± 0.0007
c_{digi}= 0.0084 ± 0.0003
Analogue case
Digital case
$1/\sqrt{E_{MC}}$ ($GeV^{-1/2}$)

What is ILC?



Electrons
Undulator
Detectors
Electron source
Positrons
Beam delivery system
Main Linac
Damping Rings
Main Linac

- SC linacs 31.5 MV/m for 11 km delivering 500 GeV collision energy (gradient is a major R&D topic – Lutz Lilje)
- Undulator-based positron source (current baseline) (major R&D topic - Jim Clarke)
- Electrons and positrons have just one damping ring each (issues of electron cloud – major R&D topic – Andy Wolski)
- Single IR, 14 mrad crossing angle
- 2 detectors operating in push-pull
[all the benefits of two detectors, other than a luminosity advantage]
- Machine must be upgradeable to 1 TeV
- 4-volume Reference Design Report plus companion document was published October 2007 – but design will continue to evolve in light of ongoing R&D

SPT technologies

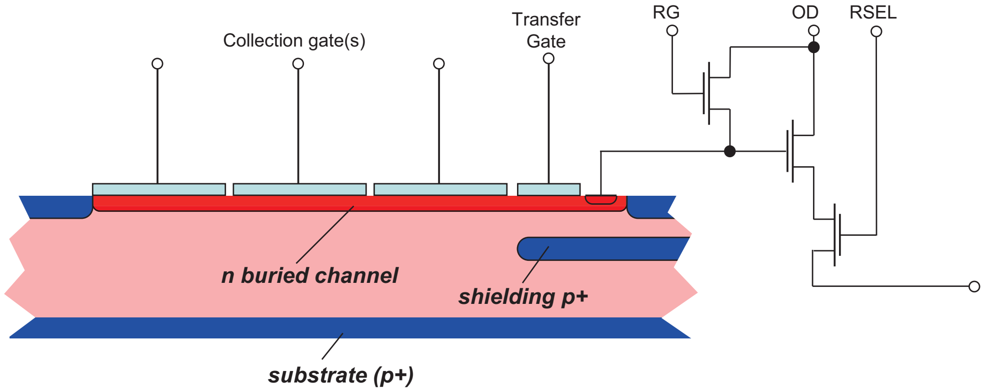
All options aim for ~15 μm precision with binary readout of 50 μm pixels

Similar area coverage to ATLAS SPT, but 5000 times more channels, 30 times less power, 20 times less material. Is this feasible?

CCD – Konstantin Stefanov

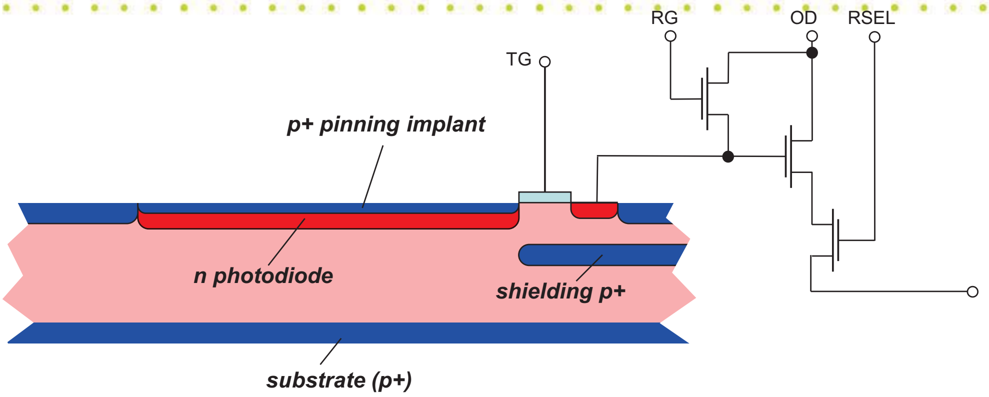
- Reasonably confident in 100% min-I efficiency, though it hasn't been demonstrated
- Total in-detector power dissipation ~600 W is fine for gas cooling
- LSST (3.2 Gpixels) being prototyped by e2V, will be a valuable 10% demonstrator

Photogate (PG + 4T) - Konstantin Stefanov



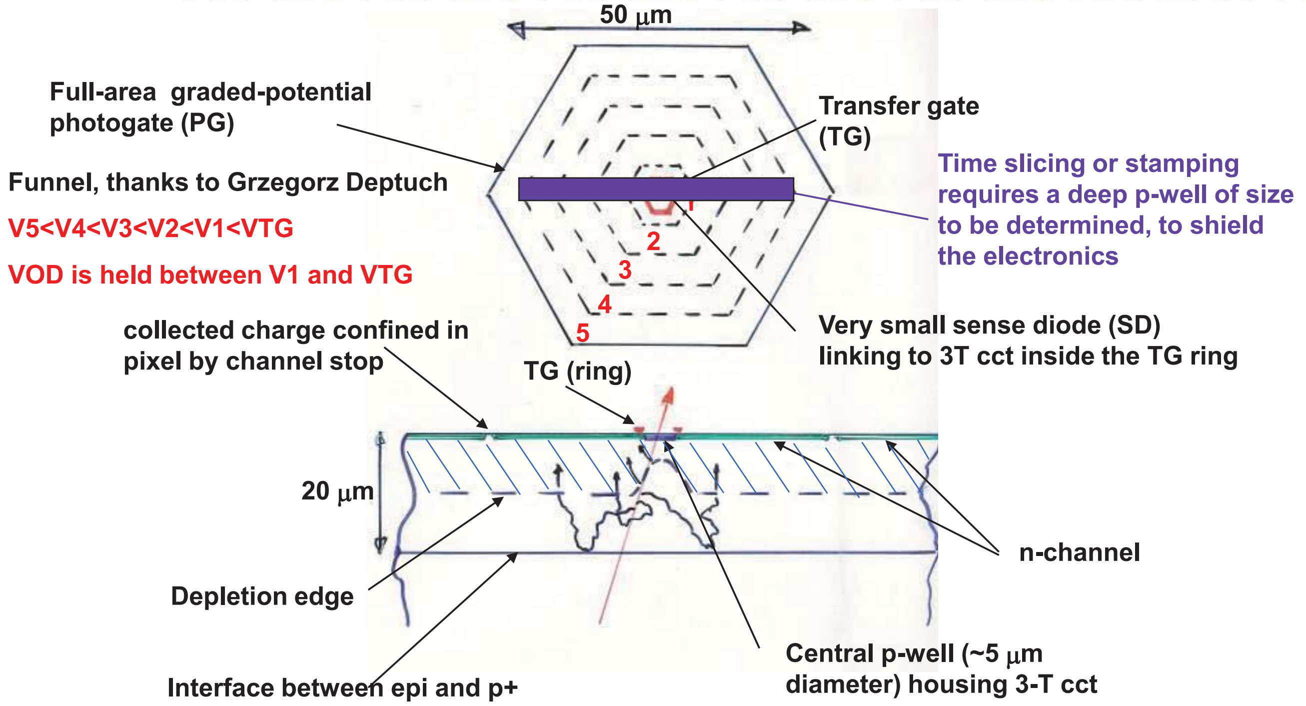
- Charge transfer allows correlated double sampling and low noise (10 e- possible)
- LCFI is developing the underpinning technology for the ISIS
- Charge transfer is fast due to funnel action (next slide)
- Possible problems with inefficient transfer due to barely buried channel and inter-gate gaps (consequences of developing a combined CCD-CMOS process)
- Hope of success with Jazz Semiconductor – currently merging with Tower

Pinned Photodiode (PPD + 4T) - Konstantin Stefanov



- PPD IP offered since ~5 years ago by numerous foundries for imaging
- Pinning implant results in fully depleted n layer
- Charge transfer gate TG decouples charge collection from sensing, permitting correlated double sampling and low noise (10 e- ENC quoted)
- Large area PPD pixels being developed at RAL
- Possible problems with *inefficient* transfer induced by small potential fluctuations in the photodiode area

PG pixel – possible layout

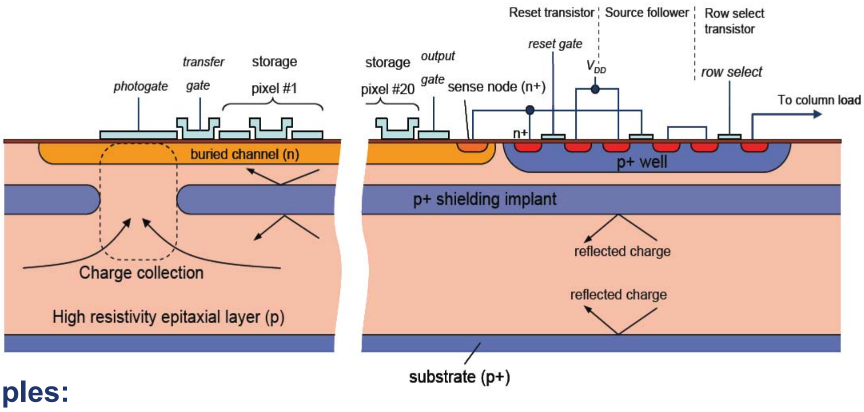


Note: Charge collection directly to TG contributes to the signal. Unwanted charge collection directly to the tiny sense diode may be negligible, so a *shielding deep p-implant may not be needed*

CPCCD – Andrei Nomerotski

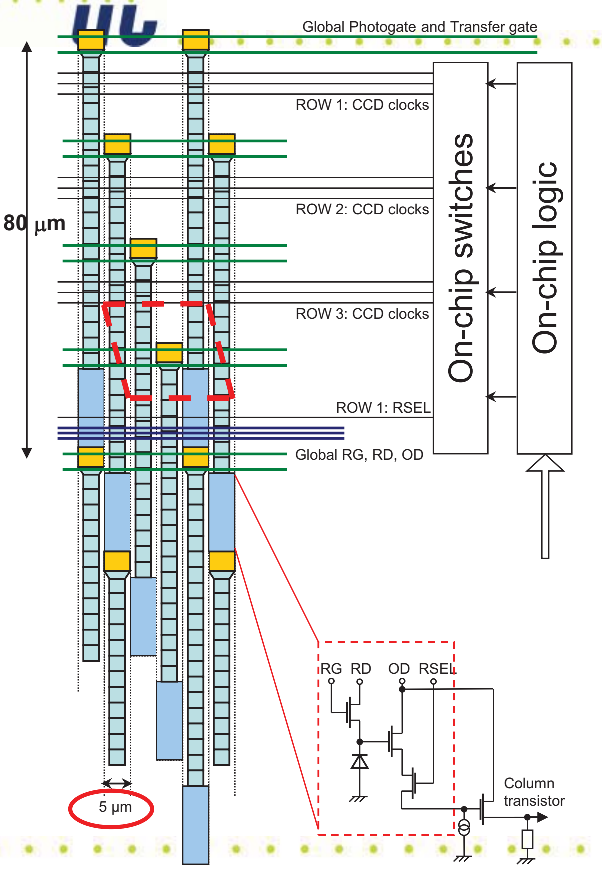
- Fast readout of CCD aiming for 50 μs frame rate
- Main novel features are column parallel readout, with bump-bond connections on 20 μm pitch to readout chip including amp, analogue CDS, ADCs, sparsification and memory
- In addition, generating the high drive current necessitated the development of special driver chips
- Possible showstoppers:
  - Unacceptable bulk of service electronics at ladder ends
  - Biggest threat is that full-scale ladders won't be made, due to lack of support from the UK funding agency (STFC)

ISIS – Andrei Nomerotski

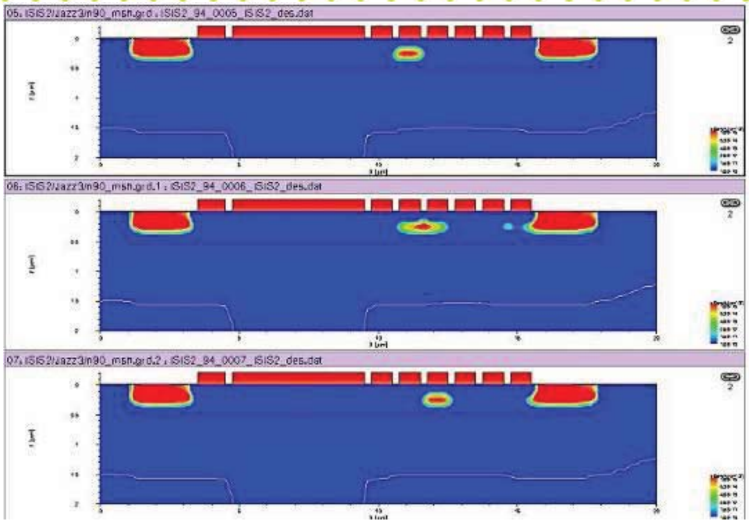


Operating principles:

1. Charge collected under a photogate
2. Charge is transferred to 20-cell storage CCD in situ, 20 times during the 1 ms-long train
3. Conversion to voltage and readout in the 200 ms-long quiet period after the train (insensitive to beam-related RF pickup)
4. As in CCDs and pinned photodiode imaging pixels (aka 4 T pixels), the output gate decouples the charge collection from the charge sensing function, which can dramatically improve the noise performance
5. 1 MHz column-parallel readout is sufficient



- ISIS combines CCDs, in-pixel transistors and CMOS edge electronics in one device: non-standard process
- Proof-of-principle device (ISIS1) designed and manufactured by e2V Technologies – works fine
- ISIS2 (a prototype close to design goals) designed at RAL (Konstantin Stefanov and Pete Murray), due for delivery from Jazz Semiconductors any day now:
  - ❖ Modified 0.18 μm CMOS process with CCD-like buried channel and deep p+ implants. Single level (non-overlapping) poly for collection and transfer gates
  - ❖ Jazz have had success with mixed CMOS-CCD pixel structures, so we have some confidence …
  - ❖ Currently 80x10 μm storage pixel: goal is 80x5, leading to 20x20 imaging pixel as shown (slightly trapezoidal)
  - ❖ If too challenging, vertical integration can come to the rescue …



3-phase, pixels ~5x3 μm (WxL)

- The ISIS concept, a prior invention for optical imaging, has led to high speed frame-burst cameras for visible light – DALSA Corp. Initially 10^6 frames/s, now developing 10^8 frames/s
- These use a pure CCD process: a challenge as been to produce a CCD structure in a CMOS process. Explored since Jan 2004 with DALSA, Tower, Zfoundry and Jazz
- Jazz is restricted to a brief BC activation step (~30 s at high temperature) and to non-overlapping gates (effective gap ~0.25 μm) in their 0.18 μm opto process – see simulation above by Konstantin Stefanov

Physics and technology of silicon detectors
(with a Linear Collider bias)

Chris Damerell (RAL)

Basic device physics can be found in the still-popular 'Vertex detectors: the state of the art and future prospects RAL-P-95-008, C Damerell 1995, available at http://hepwww.rl.ac.uk//damerell/

For further details, refer to the excellent book Semiconductor Radiation Detectors, Gerhard Lutz, Springer 1999

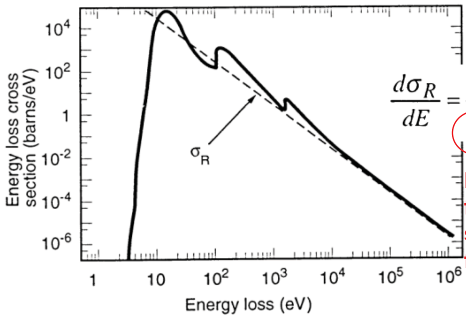
CONTENTS

- **Energy loss mechanism (ionisation – we can ignore the tiny rate of nuclear interactions)**
- **Basic device physics, relevant to silicon detectors**
- **Monolithic pixel detectors – CCDs and the recent breakthrough – charge-coupled CMOS pixels, initially for high quality cameras and now for scientific imaging, looks promising for LC vertex and tracking detectors**
- **Correlated double sampling for noise minimisation – since the 1970s for CCDs; now used with spectacular success in charge-coupled CMOS**
- **Fundamental limits to noise performance (charge-coupled-CMOS is different from CCDs)**

Why silicon for tracking detectors?

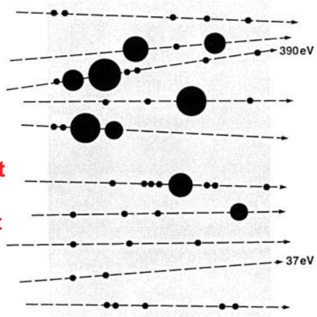
- **As 'recently' as 1975 (ie *after* discovery of J/ψ), there was little interest in tracking detectors with precision better than ~100 μm (quote from EPS Conference in Palermo)**
- **A condensed medium is obligatory for precision <10 microns (diffusion of electron cloud in gaseous detectors typically limits precision to some tens of microns)**
- **Liquids? Xenon had been tried in the early 70's but there are numerous impurity issues, affecting electron lifetime. Also, needs containers, … Is now used successfully in 'volumetric' detectors …**
- **Silicon band gap of 1.1 eV is 'just right'. Silicon delivers ~80 electron-hole pairs per micron of track, but kT at room temperature is only 0.026 eV, so dark current generation is modest, often negligible with or without modest cooling**
- **Silicon has low Z (hence minimal multiple scattering) and excellent mechanical properties (high elastic modulus). Lends itself to tracking detectors with minimal material budget**
- **Silicon is *THE* basic material of microelectronics, giving it unique advantages. Hybrid devices are acceptable in form of microstrips or large pads, but for pixel devices with possibly billions of channels, the monolithic architecture is highly desirable, and far cheaper. On-detector sparsification may almost eliminate cabling – this is usually much more important than thin silicon for minimising material budget**

Energy loss of min-I particles in Si



$$\frac{d\sigma_R}{dE} = \frac{2\pi q_e^4}{m_e c^2 \beta^2} \times \frac{1}{E^2}$$

Nuclei are relevant for multiple scattering, but not for energy loss



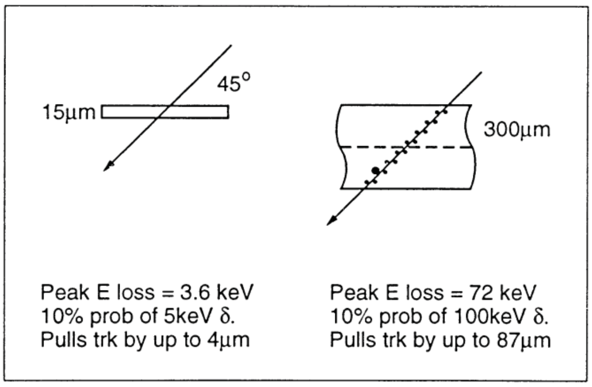
Energy deposited by min-I particles traversing 1 μn thick Si detector (Monte Carlo). Size of blob represents energy deposited, all within <1 μm of track

- **Rutherford cross-section (which assumes atomic electrons to be free) does well except for distant collisions, where the atomic binding excludes energy loss**
- **K- and L-shell electrons are liberated by hard collisions, for which the atomic binding is barely relevant**
- **M-shell (valence) electrons are excited *collectively* forming 17eV plasmons. These induce a sharp cutoff in cross-section for which the classical model has to impose a semi-empirical threshold**
- **All these primary ionisation products lose energy partly by electron-hole (e-h) generation, and partly by thermal excitation and excitation of optical phonons.**
- **Si band-gap is 1.1 eV, but on average 3.6 eV is required to generate an e-h pair, so 'efficiency' for energy loss by ionisation is ~30%**
- **This 'pair creation energy' W depends weakly on temperature (increases by 4% from room temp down to 80K), but otherwise it applies over a wide range of excitations, including high energy particles, x-rays and UV photons. For visible light, it's of course different …**

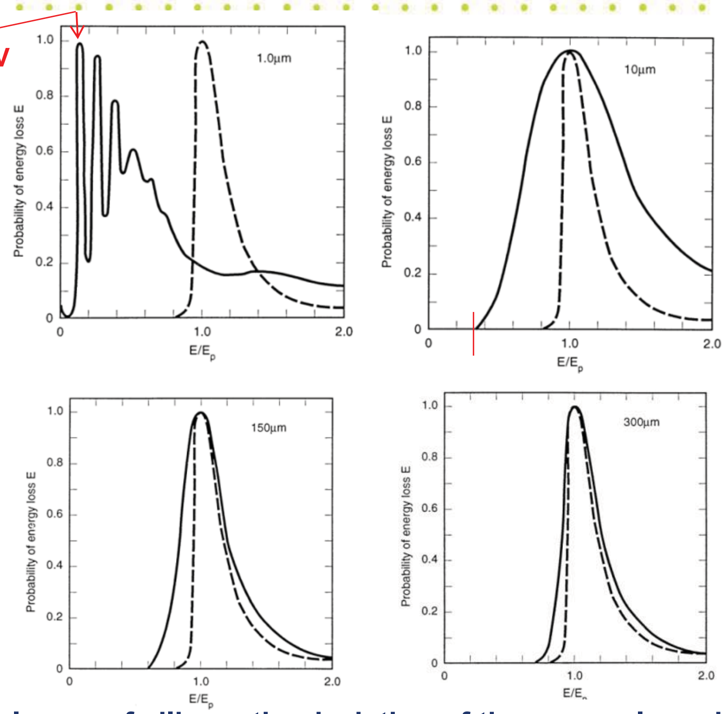
Electrons	Collision probability per micron
K (2)	8.8 x 10^{-3}
L (8)	0.63
M (4)	3.2

Total: 3.8 primary collisions /μm

- **For precise track reconstruction, it is desirable to minimise the active thickness of silicon, hence the probability that fluctuations in energy loss can seriously pull the position of the reconstructed cluster in the detector plane**
- **In principle this can be avoided by excluding the tails with large energy loss (if it is measured) but one usually lacks the required level of redundancy in detector planes**

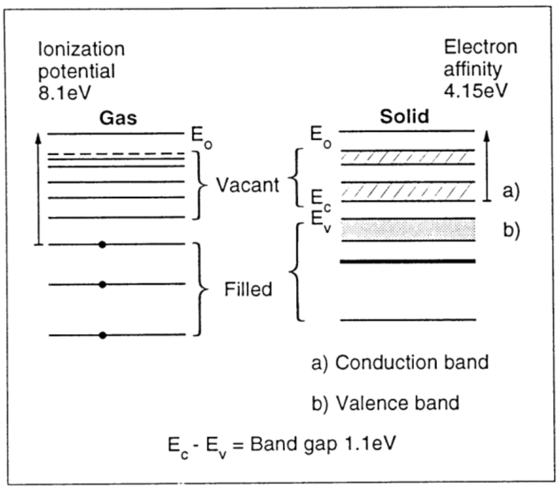


One phonon of 17 eV



- **For thin active layers of silicon, the deviation of the energy-loss distribution from Landau is dramatic. Even for 10-20 micron thickness, need to be careful with noise performance/threshold settings in order to achieve efficient min-I detection**

Semiconductor physics (bare essentials)

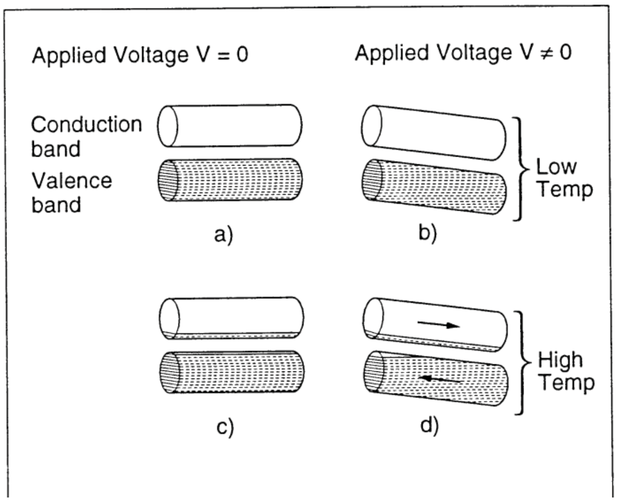


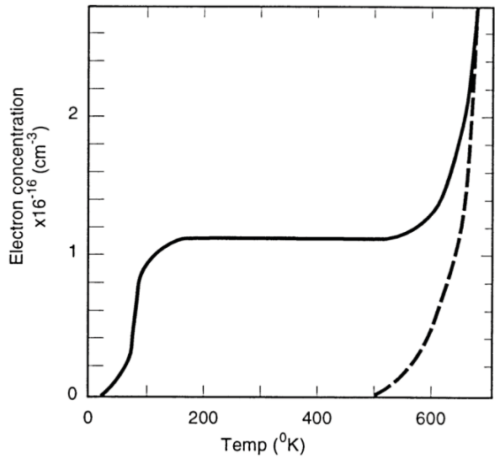
- **Insulator: conduction band several eV above valence band**
- **Conductor: conduction band overlaps with valence band**
- **Semiconductor: conduction band close enough that at room temp, significant number of electrons are excited from valence to conduction band**
- **Extrinsic (doped) semiconductor: implanted/activated impurities provide donor levels close to conduction edge, or acceptor levels close to the valence edge**
  - **These are called n- and p-type material - free electrons and holes respectively**

- **Fortuitously, SiO_2 has a band gap of 9 eV – a perfect insulator, unless you make it too thin (few nm), in which case currents due to electron tunneling can be significant**

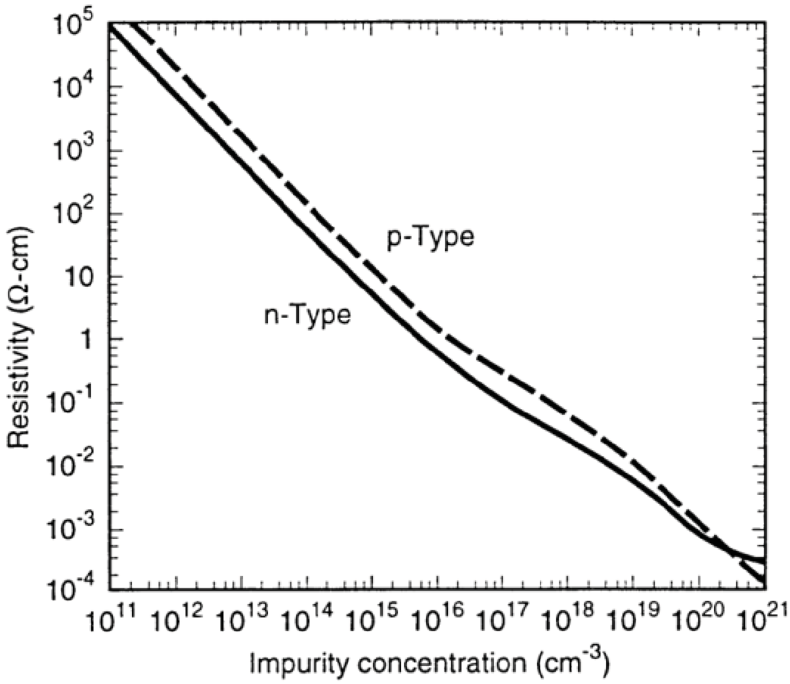
- **At room temp, Si resistivity is 235 kOhm.cm**

Undoped and doped silicon

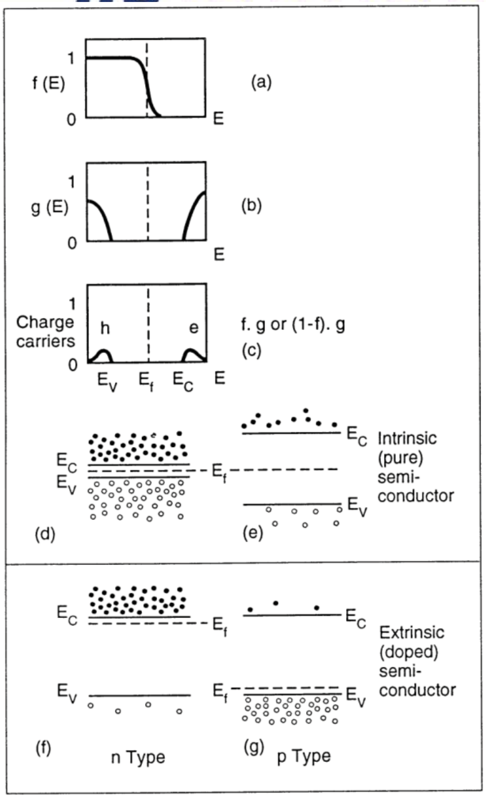




- Intrinsic (undoped) silicon becomes a good conductor only at ~600 C
- By doping with donor or acceptor atoms, conduction is achieved right down to ~100 K or below
- Doping can be done during crystal growth (bulk), or when growing an epitaxial layer of typically tens of μm thick, or during device processing, with patterning precisely controlled by photolithography/photoresist
- Next slide: resistivity as function of dopant concentration for n-type (arsenic) and p-type (boron) material



- For active layer, may be desirable to have resistivity in region of 10 kΩ cm
- Implies dopant concentrations ~10^{12} cm^{-3}, ie impurity levels of ~2 in 10^{11} . Amazingly, the manufacturers can provide this, in bulk and in epitaxial material



- **Fermi-Dirac distribution fn: probability that a state of energy E is filled by an electron:**

$$f_D(E) = \frac{1}{1 + \exp\left(\dfrac{E - E_f}{kT}\right)}$$

- ***E_f*, the Fermi level, is the energy level for which the probability of occupancy = 50%**
- **Hole occupancy in valence band is given by (1-*f_D*)**
- **Charge carrier concentration is given by product of the occupancy and the density of states *g(E)***
- **Sketches conventionally show only the mobile charge carriers. However, charge neutrality in the material is generally satisfied for homogeneous samples, with or without current flow.**
- **Beyond these, one would be discussing situations with space-charge effects, typically *depleted* material**

- **Cutting a long story short, carrier concentration in doped material is given by:**

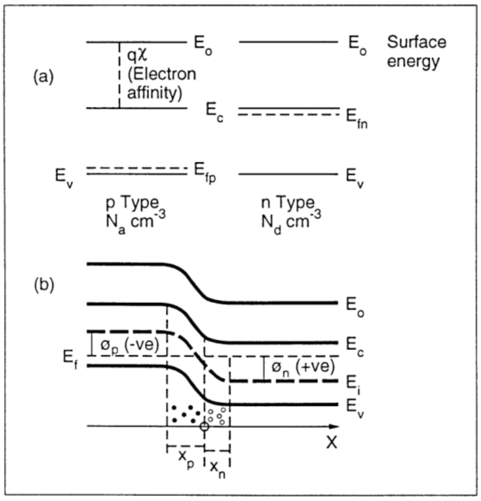
$$\left.\begin{aligned} n &= n_i \exp\left(\frac{E_f - E_i}{kT}\right) \\ p &= n_i \exp\left(\frac{E_i - E_f}{kT}\right) \end{aligned}\right\}$$

$$pn = n_i^2 = N_c N_V \exp(-E_g / kT) \textit{ just as for intrinsic material.}$$

- ***E_i* is very close to mid band-gap, so as the dopant concentration pulls *E_f* either above or below that level, the concentration of electrons or holes (majority carriers) explodes, and the concentration of the opposite sign carriers (minority carriers) collapses, and for many purposes can be considered to vanish entirely**
- **For silicon, the temperature dependence of *n_i* is given by $T^{3/2}\exp(-E_g/2kT)$; ie at room temp a doubling for every 8 C temperature rise**

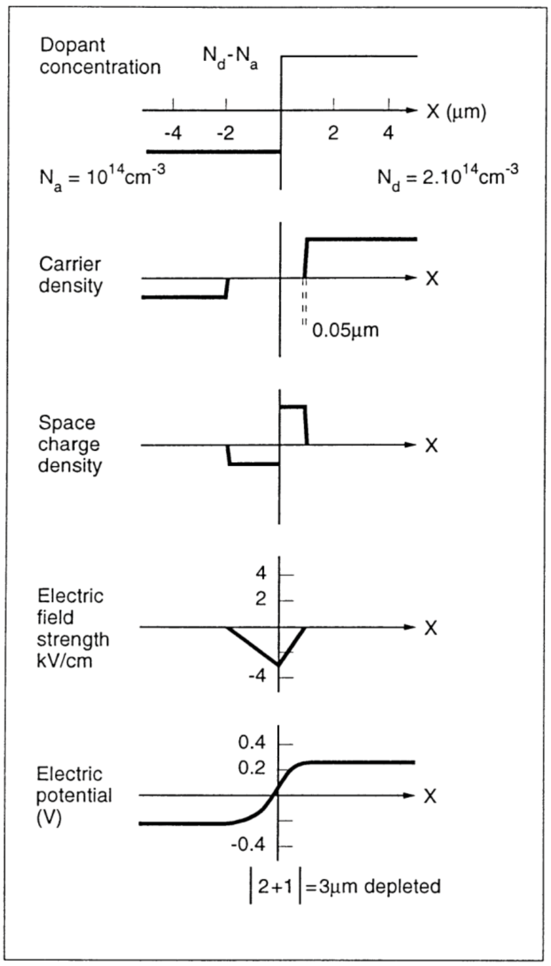
The *pn* junction

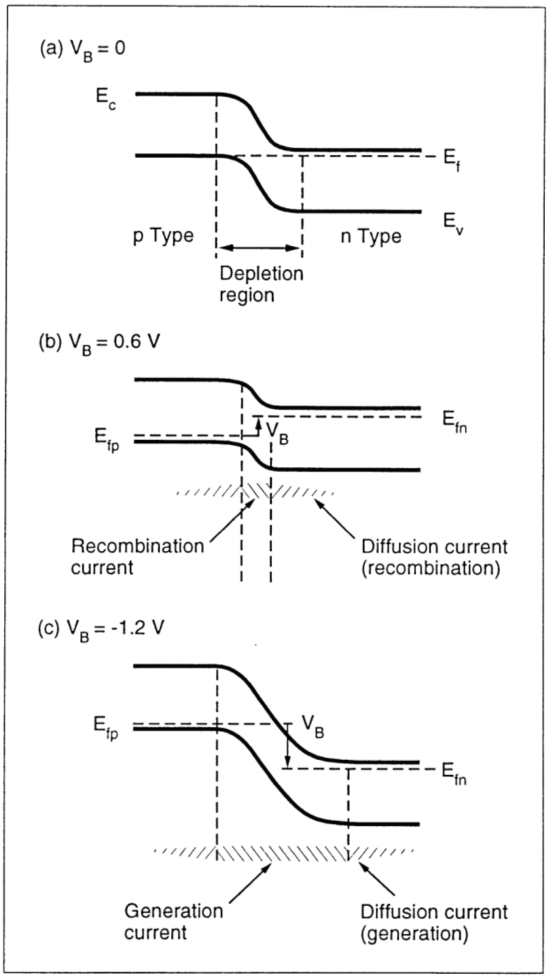
- Think of bringing two pieces of doped Si, one p-type, one n-type into contact, both grounded by a metal contact*
- Charge carriers diffuse, electrons one way, holes the other, to 'fill the vacuum'
- This creates a depletion region (space charge) across the junction
- Charge flow continues till the Fermi level is constant across the junction (condition for equilibrium)
- Majority carriers are repelled by the potential barrier, minority carriers are attracted across it
- In thermal equilibrium, exactly as many electrons from the n-region overcome the barrier as electrons from the p-region are pulled across it. Vice versa for holes
- Note that there is no NET space charge. If one dopant concentration is higher than the other, the depletion region is correspondingly shallower – see next slide



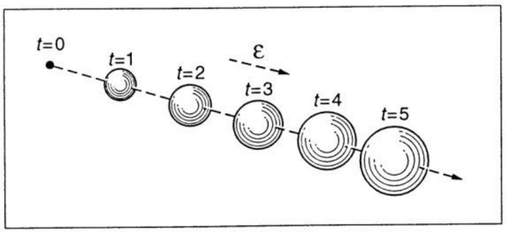
•FINE PRINT: There's a subtle point of work functions, Schottky diodes, electron tunnelling – discuss later if interested

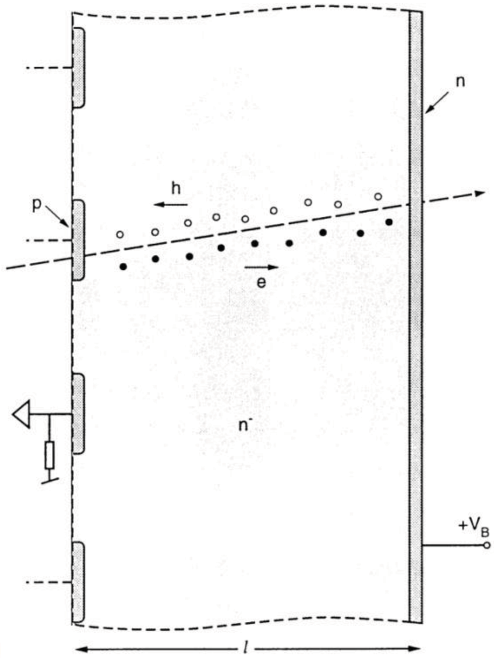
- If one now imposes a potential difference across the junction, one will either diminish or increase the thickness of the depletion region (fwd or reverse biased diode) – see next slide





- Now you have all the tools you need to understand the essentials of silicon detectors …





- Typical microstrip detector: high resistivity n bulk, heavily doped p-strips, heavily doped back contact
- Reverse bias creates partial depletion of the p-strips, full depletion of the bulk
- Charge collection is by drift and diffusion
- Signal starts to form as soon as the carriers begin to move: a fast and slow component seen symmetrically on both electrodes
- Readout is typically by local electronics ('front-end chip'), wire bonded strip by strip
- With ~300 μm thick detector, min-I signal is clearly seen above noise (simple discriminator)
- With this approach, there is nothing to gain from a submicron front-end cct; on the contrary, optimal performance has $C_{sensor} \sim C_{detector}$

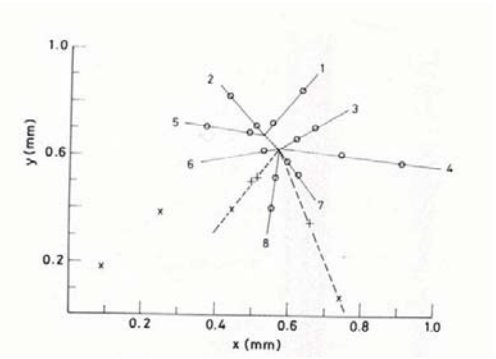
- Note one essential feature: signal charge is collected on a reverse-biased diode (effectively a capacitor), and is sensed by the induced voltage change

- This is so standard for HEP detectors that some people tend not to consider alternatives – it is the operating principle of microstrip detectors, hybrid pixels and all the monolithic 3T CMOS pixels that have so far been deployed in HEP detectors

- However, 3T pixels suffer from high noise and high dark current, which has limited their applicability for scientific applications

- One can in principle do MUCH better regarding these performance parameters, as has been seen in CCDs since the 1970s. This approach was 'exported' to CMOS pixels for high quality cameras around 1992 and is now under rapid development for scientific CMOS pixel sensors

Monolithic pixel detectors



- **For LC vertexing, there is no longer any debate. Unanimity was achieved as result of a talk by Chris Bowdery at LCWS 1993 in Hawaii. Prior to that, microstrips ('good enough for DELPHI' were pushed by some)**
- **For LC tracking, the suggestion was launched at the Asian LC workshop in Sendai in 2008, but is not yet in anybody's baseline.**
- **Meanwhile, for the rest of the world of digital cameras, scientific imaging, etc, the pace of progress is remarkable …**

Historical/technical overview (simplified)

Charge-coupled devices (CCDs)

devices up to wafer-scale, wide range of pixel sizes, low dark current* and excellent noise performance, slow readout

Wide range of scientific applications

CMOS active pixels (MAPS)

3T pixels restricted to small pixel sizes, relatively high dark current* and poor noise performance, fast readout

Limited scientific applications

Charge-coupled CMOS pixels

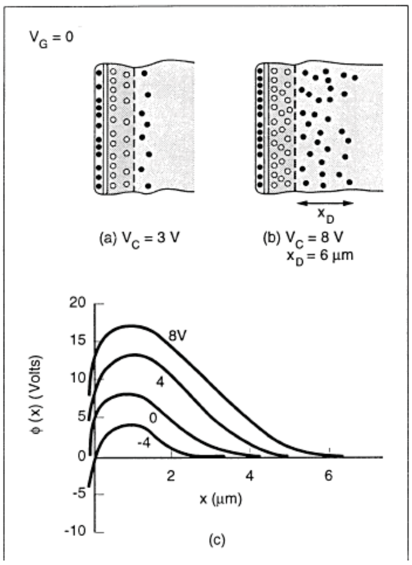
wide range of pixel sizes, low dark current and excellent noise performance, fast readout

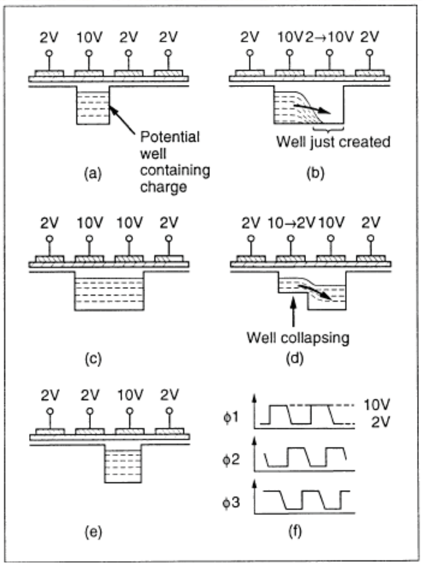
Potentially wide range of scientific applications

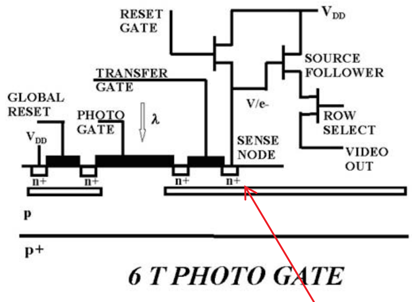
*** 1-10 pA/cm^2 (CCD) cf 200-500 pA/cm^2 (3T CMOS)**

Omitted: DEPFET, which is an MPI Halbleiterlabor in-house charge-coupled non-CMOS architecture with special properties and wide scientific applications

From CCDs to charge-coupled CMOS pixels







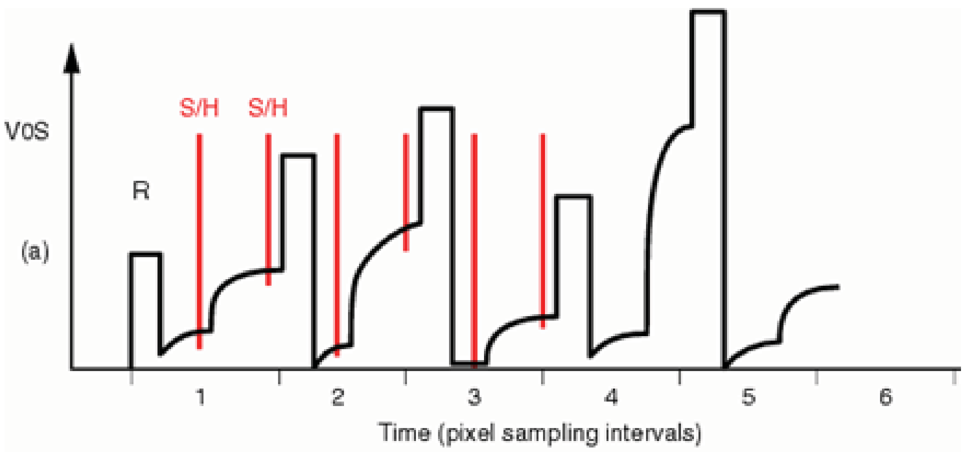
Janesick 2002

p+ shielding implant

- **There are several variants, but in all cases, the key is:**
  - **Collect signal charge on a fully-depletable structure (PG or PPD) having relatively large capacitance. Shield in-pixel electronics with a deep p-implant**
  - **Sense 'baseline' voltage on gate of miniature transistor having minimal capacitance**
  - **Transfer entire signal charge to this gate and sample again, *promptly***
  - **Voltage difference is CDS measurement of the signal**

Correlated double sampling (CDS)

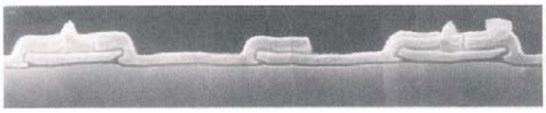
[Possible only for charge-coupled pixels]



Baseline settles to a different level after each reset, due to *kTC* noise. Entire signal charge is transferred to the output node between the two 'legs' of the CDS.

This eliminates reset noise, fixed-pattern noise, dark-current-related noise, and suppresses pickup – low and high frequency. It enables astronomers to achieve few-electron noise performance with long exposure times, and particle physicists to make efficient trackers with ~20 μm thickness of active silicon

• Advantages are obvious, so why has the CMOS pixel community been stuck with 3T pixels for so long?

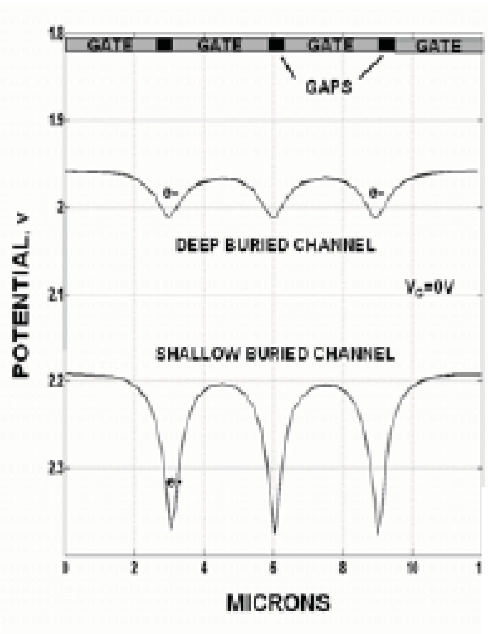


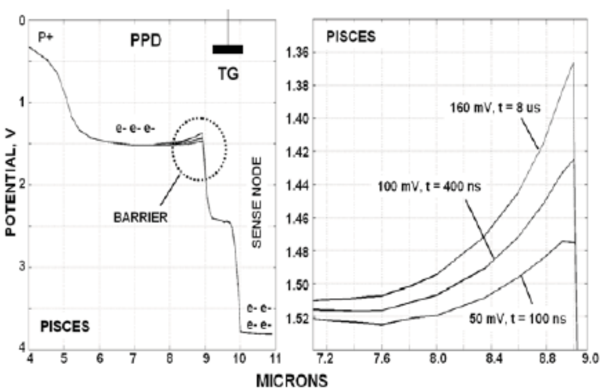
• D Burt, many years ago: 'The literature is littered with failed attempts …' Why was this difficult, and how has the problem been solved?

• Unlike with CCDs, every layer of a CMOS device needs to be precisely planarised, or the photolithography for the next layer will be out of focus

• For metal layers, planarisation is achieved by the technique of damascening

• With 0.18 μm CMOS, an intergate gap of 0.25 μm can be achieved with a single poly layer, and this is (just) adequate





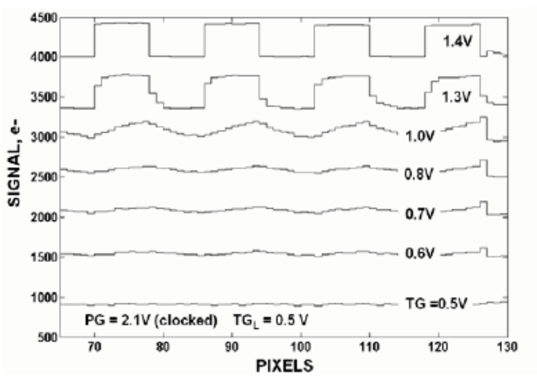
• Simulations for BC charge-coupled CMOS (Jim Janesick 2009)

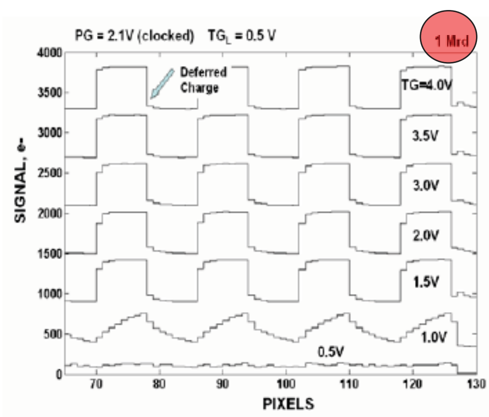
• Similarly encouraging results even for gates as short as 1 μm (Konstantin Stefanov 2007)

• However, short-channel effects and fringing field effects are a big issue (George Seabroke 2009)

- Charge-coupled CMOS pixels were first developed for commercial products - high quality cameras
- For scientific applications, there are numerous developments under way:
  - Jim Janesick with Jazz Semiconductor
  - RAL/Oxford with Jazz Semiconductor (ISIS)
  - James Beletic with Teledyne Imaging Sensors
  - Oregon/Yale with Sarnoff (chronopixels)
  - e2V with Tower Semiconductor
  - Spider Collaboration with ‘Foundry A’ (Fortis)
  - Andor/Fairchild/PCO (sCMOS) – Press release 15 June, they list 23 scientific application areas
  - And probably many others …
- Numerous design variants, 4TPPD, 5TPPD, 4TPG, 6TPG etc. However, the key in all cases has been to develop a working charge-transfer capability within the CMOS process

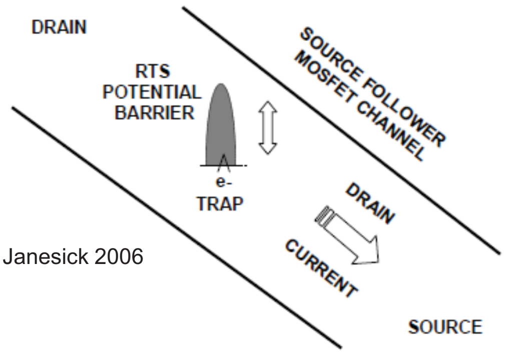
- Due to the small pixel sizes, even surface channel devices perform well
- Usable up to 1 Mrad ionising radiation (need 2.6 V higher TG amplitude), and this is only the beginning

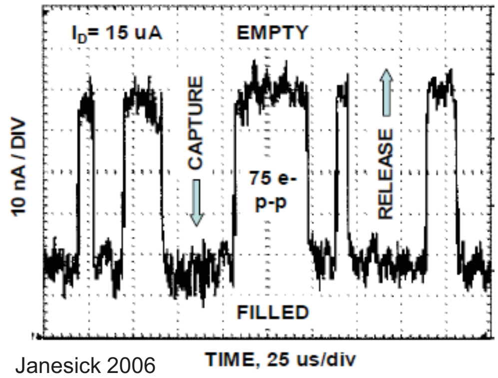




Janesick 2009

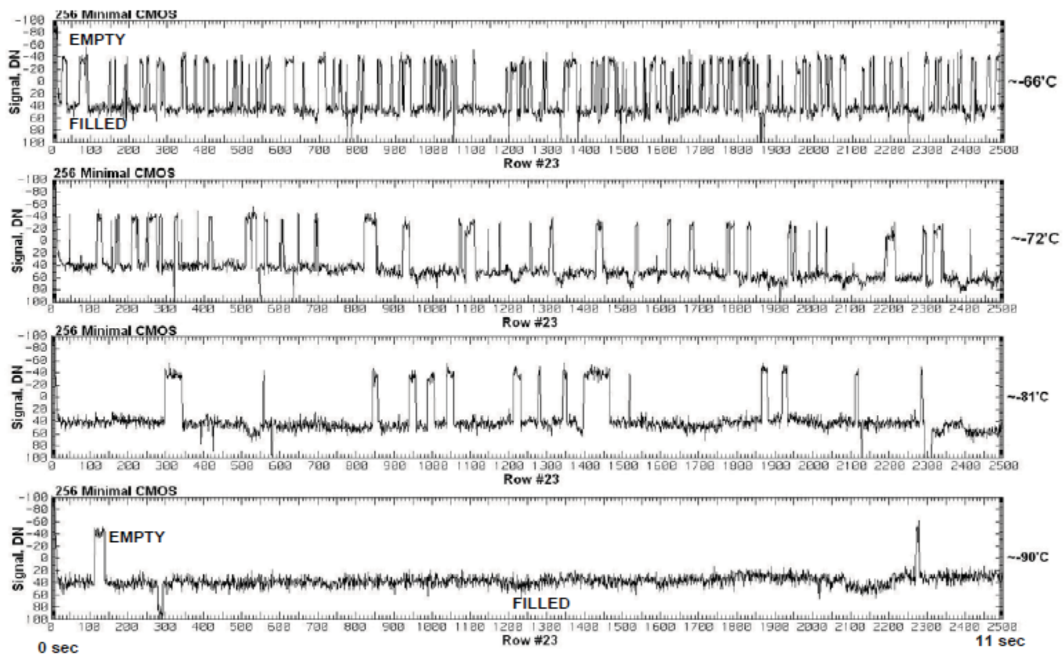
RTS noise





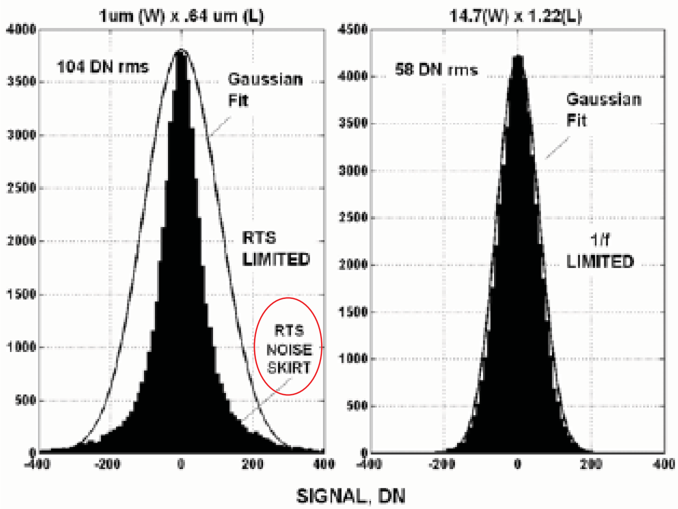
Note: These fluctuations amount to only 0.3% of the drain current

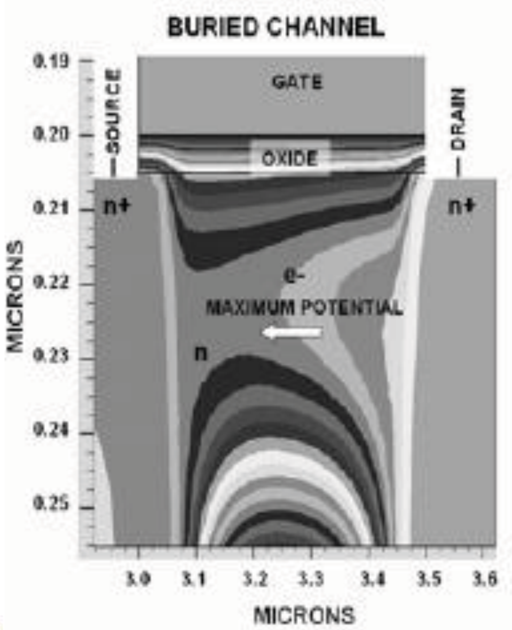
- This is the dominant residual noise source in charge-coupled CMOS pixels
- As with CCDs, transistor noise can be much reduced by using a buried-channel MOSFET for the source follower (but not completely eliminated, due to the presence of bulk traps)



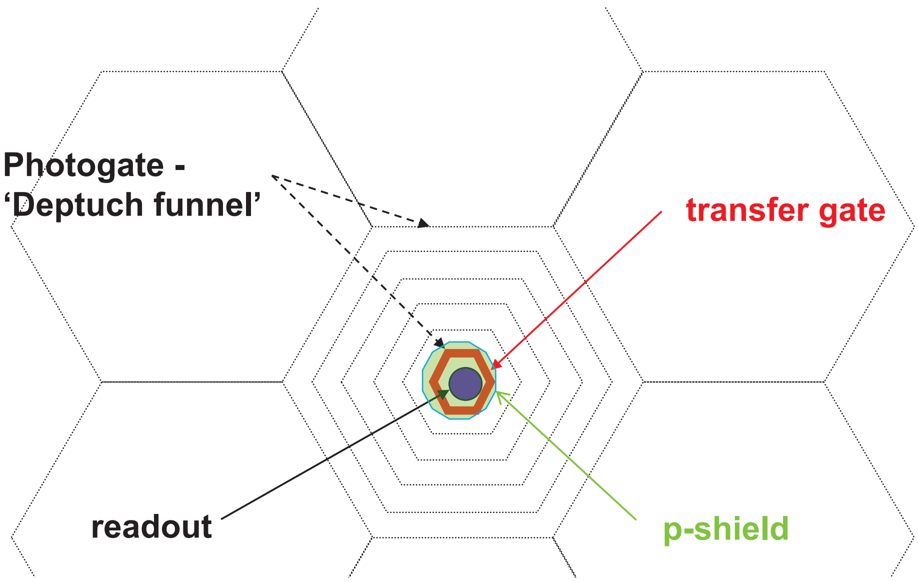
Janesick 2006

Despite this behaviour, there is *nothing* (as regards noise performance) to be gained by cooling!





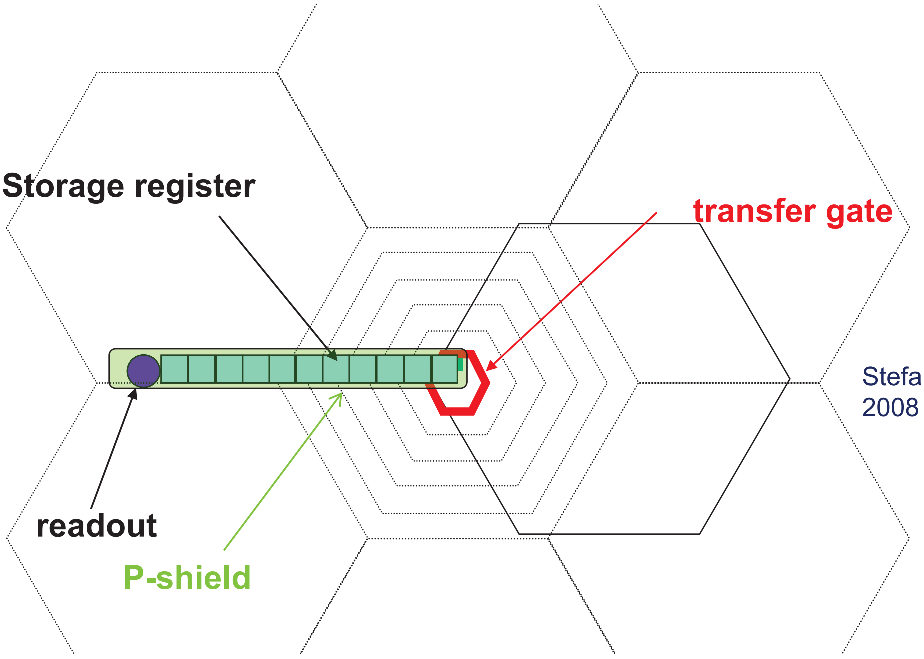
Silicon Pixel Tracker for ILC – a possible architecture



SPT pixels (~50 μm diameter):

- 3 tiny transistors inside ring-shaped transfer gate in p-well
- ‘Deptuch funnel’ – need only ~50 mV per stage (and couldn’t be much higher, if one uses a 0.18 μm process, limited to 5 V) [dual gate thickness, 12 nm and 5 V, 4.1 nm and 1.8 V]
- What if time slicing is required?

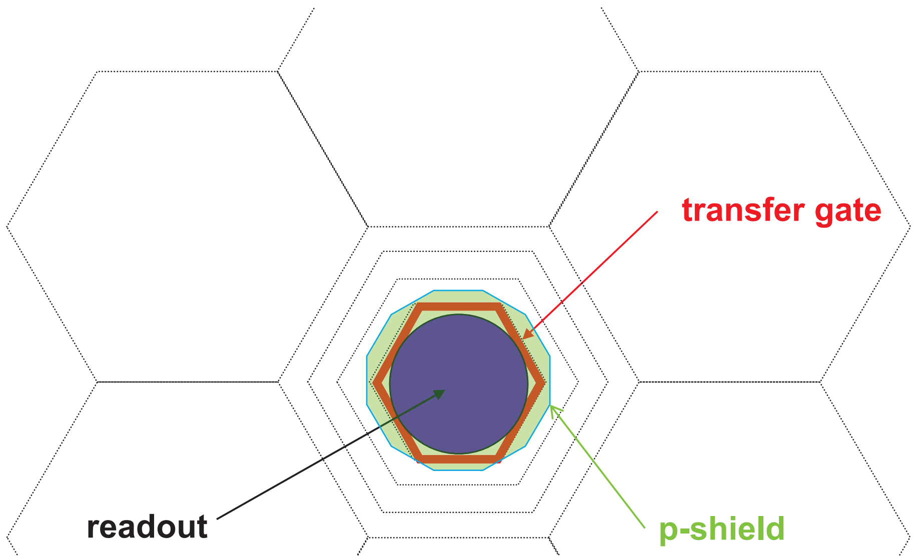
Silicon Pixel Tracker for ILC – forward region



Stefanov, Sendai LC wkshop, 2008

- Also of interest for fast-frame burst camera for X-ray imaging at 4th generation light sources (LCLS and XFEL)
- Fully deplete (currently 30 kΩ-cm epi is available)
- Back-illuminate: soft X-rays: direct conversion
  hard X-rays: via columnar CsI

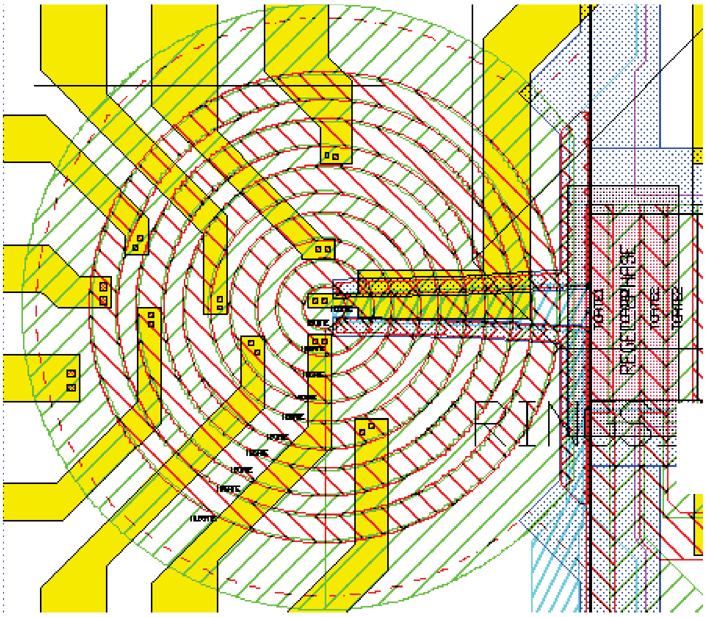
Silicon Pixel Tracker for ILC – if full time-stamping were needed



SPT pixels (~50 μm diameter):

- in-pixel discriminator and time stamp for binary readout, possibly with multi-hit register
- could even contemplate in-pixel ADC, but that is probably science fiction
- Between trains, apply data-driven readout of hit patterns for all bunches separately
- p-shield ensures full min-I efficiency, even if a large fraction of the pixel area is occupied by CMOS electronics
- The showstopper could be the power dissipation per unit area, and impact on layer thickness

- It turns out that both funnel and register have been fabricated by e2V for confocal microscopy: 100% efficient for single photoelectrons – noiseless, by using LLL (L3) linear register



Diameter of outer active ring ~ 100 μm

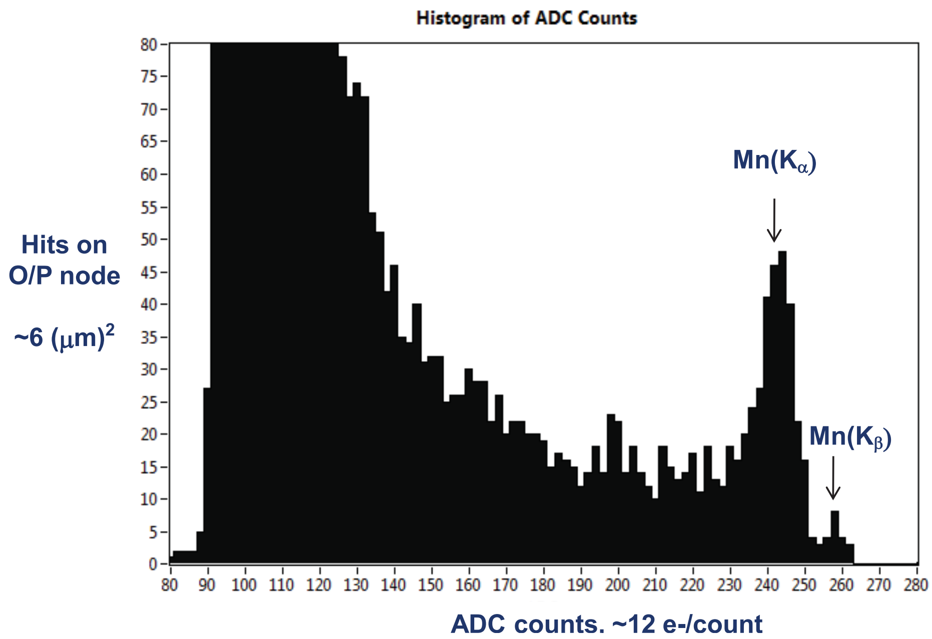
[David Burt, e2V technologies]

Conclusions and Outlook

- Monolithic silicon pixel detectors took over from photographic film in the '90s, for visible light and x-ray imaging in astronomy
- Their development for particle physics has been slow, but with some exceptions, these detectors are likely to evolve as the technology of choice for vertexing and tracking in particle physics (my opinion)
- It hasn't always been easy – note reactions of experts in our field circa 1979
- It still wasn't accepted for vertexing as late as 1982; remember the SLC baseline just 8 yrs before startup (bubble chamber) and even until 1993 for ILC (Bowdery, Hawaii). 'What was good enough for LEP will be good enough for ILC'. 'Just take DELPHI'
- Even in 2009, silicon pixels aren't widely considered for tracking at ILC or CLIC, due largely to entrenched opinions. They aren't the baseline in any of the LOIs. 'The better is the enemy of the good'. Same story as we first encountered for LC vertexing
- Furthermore, there's always room for a completely new idea. Don't be discouraged if you have one, and it also meets with initial disapproval. There is plenty of time to revise the 'baseline designs' for the detector concepts
- R Feynman: 'In any technology, truth must take precedence over public relations, for Nature cannot be fooled.'
- While totally new ideas can never be ruled out, the rapidly expanding silicon technology, which embraces microelectronics and camera chips, provides us with a powerful toolkit, free of charge to the HEP community. Where appropriate, we would be wise to take advantage of it

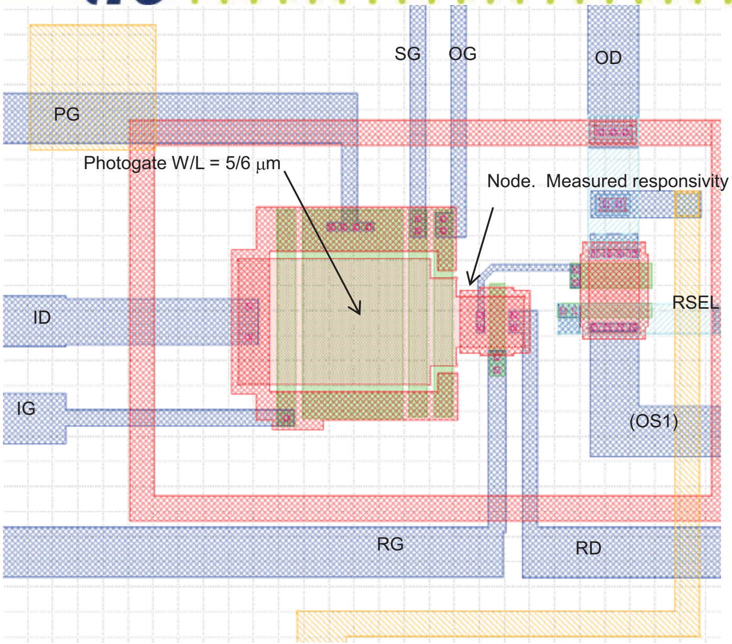
backup

^{55}Fe Signal - Gary Zhang – 4 June 2009



- **Shaping time matched to 7 MHz readout**
- **in 30 years working with fast readout CCDs, we never resolved these peaks**
- **Promises micron precision in centroid finding for MIPs with approximately normal incidence**

ISIS-2 buried channel test structure



- Short-channel and fringing field effects are large. Former have been simulated, latter still under way …
- Combining results with this BC structure, and Janesick's 130-element SC register, we can see that the ILC technical requirements are already in hand
- The most urgent need now is to develop the ISIS for near-term SR applications

SLC Experiments Workshop 1982, just 8 years before start of SLC

Who knows what the future holds? Beware of premature technology choices for ILC!

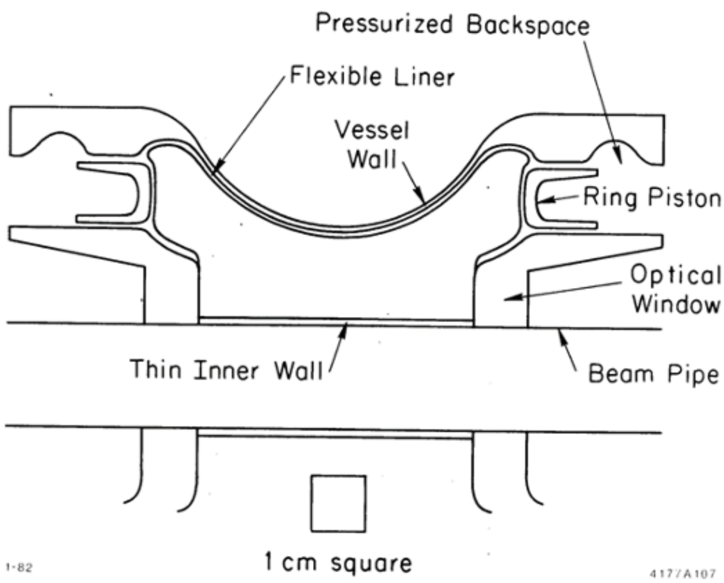
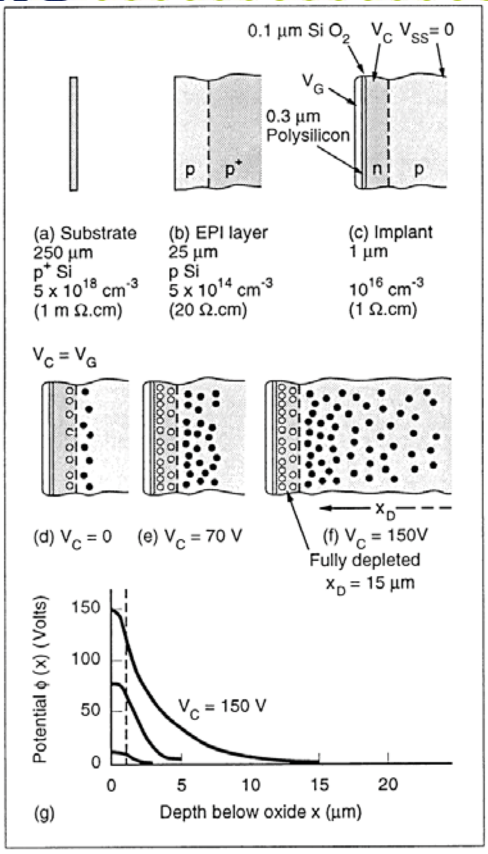
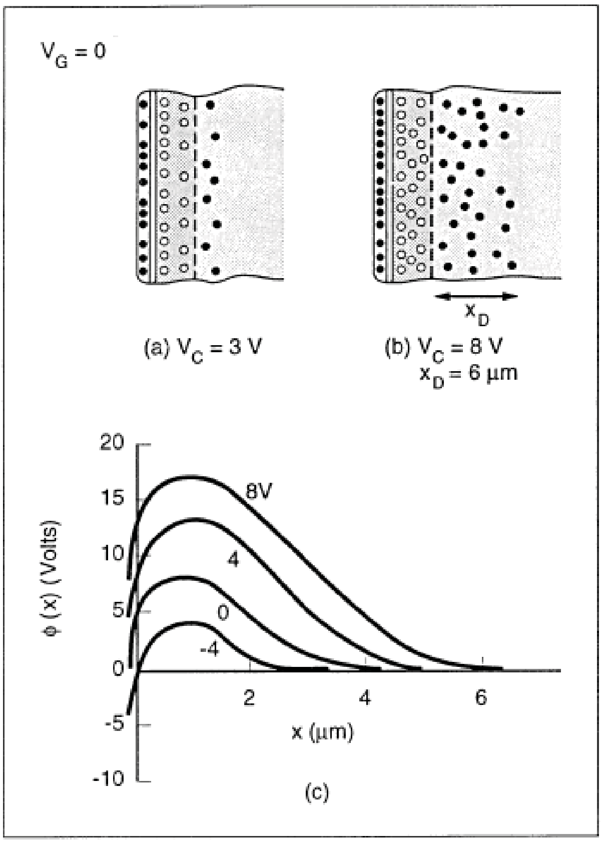
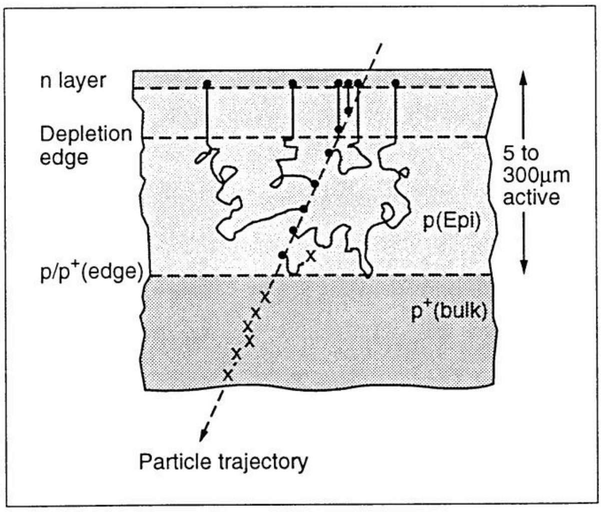
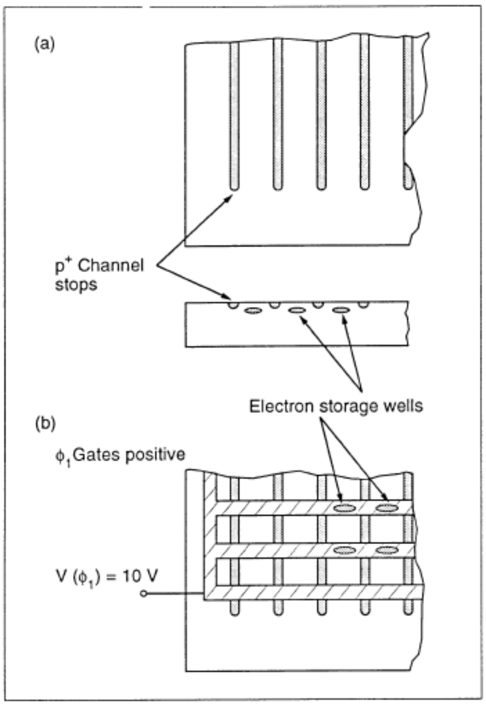


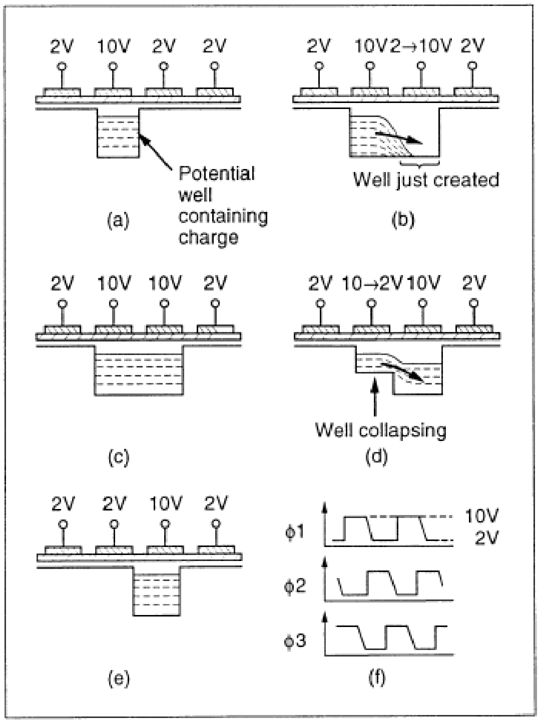
Fig. 7. Conceptual design of a propane bubble chamber vertex detector.

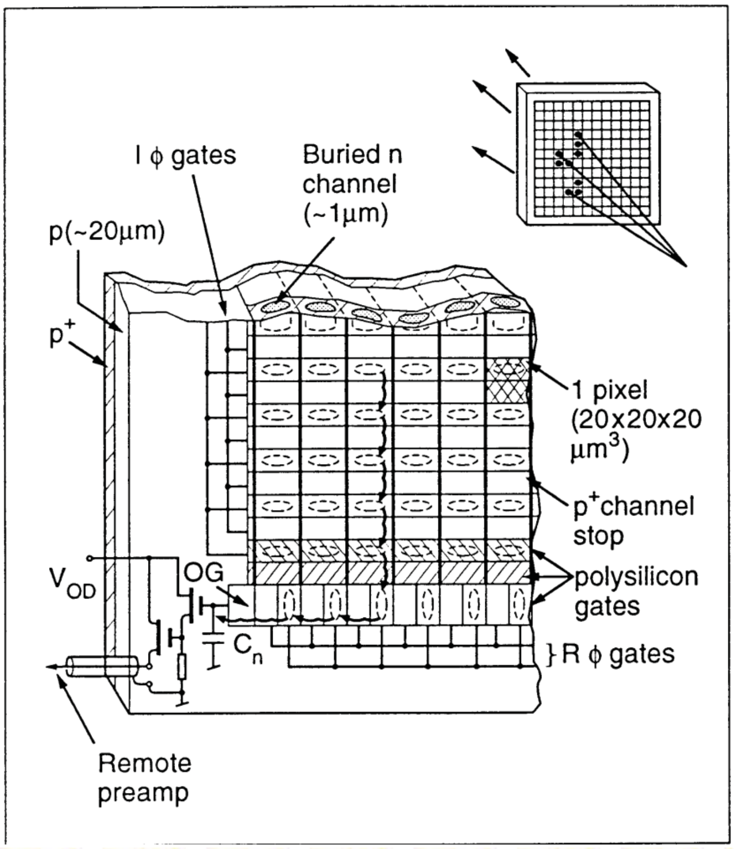

0.1 μm Si O_2
V_C V_{SS}= 0
V_G
0.3 μm Polysilicon
p p$^+$
n p
(a) Substrate 250 μm p$^+$ Si 5 x 10^{18} cm^{-3} (1 m Ω.cm)
(b) EPI layer 25 μm p Si 5 x 10^{14} cm^{-3} (20 Ω.cm)
(c) Implant 1 μm 10^{16} cm^{-3} (1 Ω.cm)
V_C = V_G
x_D
(d) V_C = 0
(e) V_C = 70 V
(f) V_C = 150V Fully depleted x_D = 15 μm
Potential φ (x) (Volts)
150
100
50
0
V_C = 150 V
0
5
10
15
20
Depth below oxide x (μm)
(g)

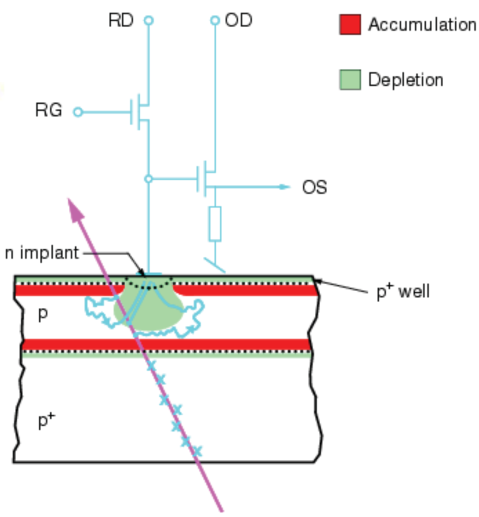

V_G = 0
x_D
(a) V_C = 3 V
(b) V_C = 8 V x_D = 6 μm
20
15
10
5
0
-5
-10
φ (x) (Volts)
8V
4
0
-4
2
4
6
x (μm)
(c)


n layer
Depletion edge
p/p$^+$(edge)
5 to 300μm active
p(Epi)
p$^+$(bulk)
Particle trajectory


(a)
p^+ Channel stops
Electron storage wells
(b)
ϕ_1 Gates positive
V (ϕ_1) = 10 V


2V 10V 2V 2V
Potential well containing charge
(a)
2V 10V2→10V 2V
Well just created
(b)
2V 10V 10V 2V
(c)
2V 10→2V 10V 2V
Well collapsing
(d)
2V 2V 10V 2V
(e)
φ1
φ2
φ3
10V
2V
(f)


I φ gates
Buried n channel (~1μm)
p(~20μm)
p^+
1 pixel (20x20x20 μm^3)
p^+channel stop
polysilicon gates
V_{OD}
OG
C_n
} R φ gates
Remote preamp



❑ We can repeat this on the top surface – here the *p*-well can be used to implant structures (notably n-channel transistors), 'monolithic' with respect to the detector layer below

❑ Positively biased n implants (reverse-biased diodes) serve to collect the signal charges, partly by diffusion, partly by drift in depleted regions created in the *p*-type epi layer

❑ Overlaying dielectric layers, and photolithographically patterned metal layers complete the toolkit for interconnecting the circuit

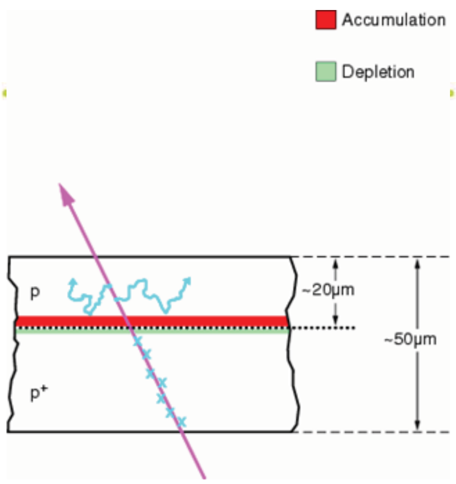
❑ Here you have the essentials of a 3T MAPS (monolithic 'active' pixels sensor, having transistors within the pixel; in contrast to 'passive' CCDs)

❑To learn about all the beautiful options for ILC vertex detectors, refer to the website of the ILC Detector R&D Panel at https://wiki.lepp.cornell.edu/wws/bin/view/Projects/WebHome

Minority carrier diffusion length

~ 200 μm

~ 0.1 μm



What epi-layer thickness?

Prefer it thin, to avoid losing precision for angled tracks

But not too thin, or lose tracking efficiency

20 μm is 'about right'

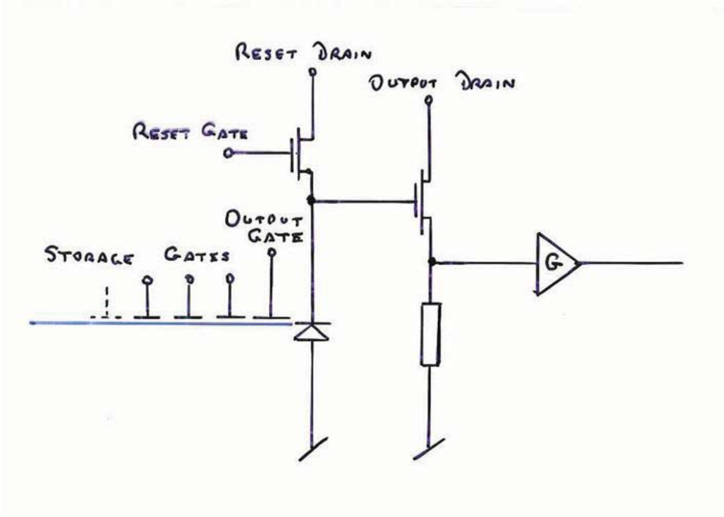
❑ Imagine *p* and *p+* material brought into contact at same potential

❑ Holes pour from *p+,* leaving a negative space-charge layer (depletion) and forming a positive space charge layer in the p material (accumulation)

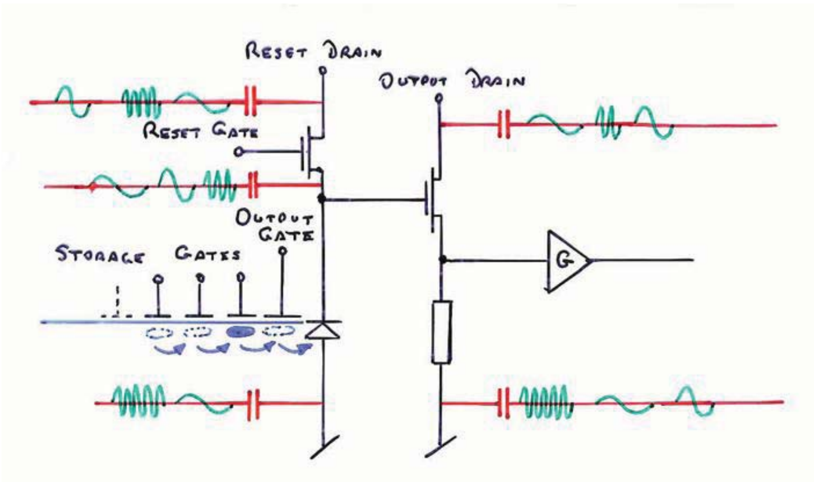
❑ This space-charge must of course sum to zero, but it creates a potential difference, which inhibits further diffusion of majority carriers from *p+* to *p* and *incidentally* inhibits diffusion of minority carriers (electrons) from *p* to *p+*

❑ This barrier is thermally generated, but the 'penetration coefficient' is temperature independent, and is simply the ratio of dopant concentrations. eg 0.1/1000, so 10^{-4} - this interface is an almost perfect mirror!

Typical example: ideal CCD



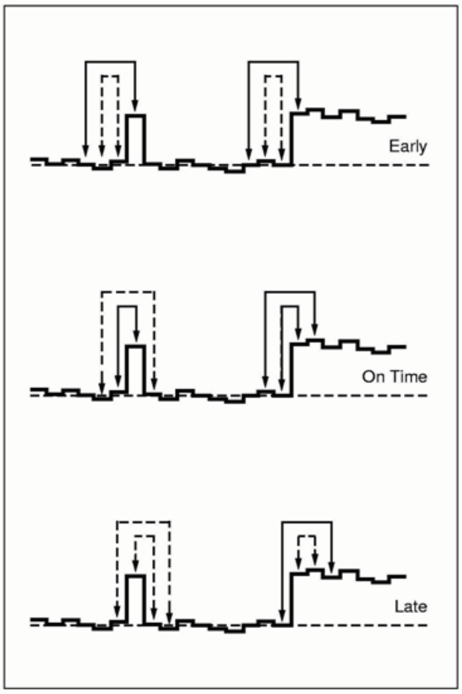
Reality, during the bunch train:



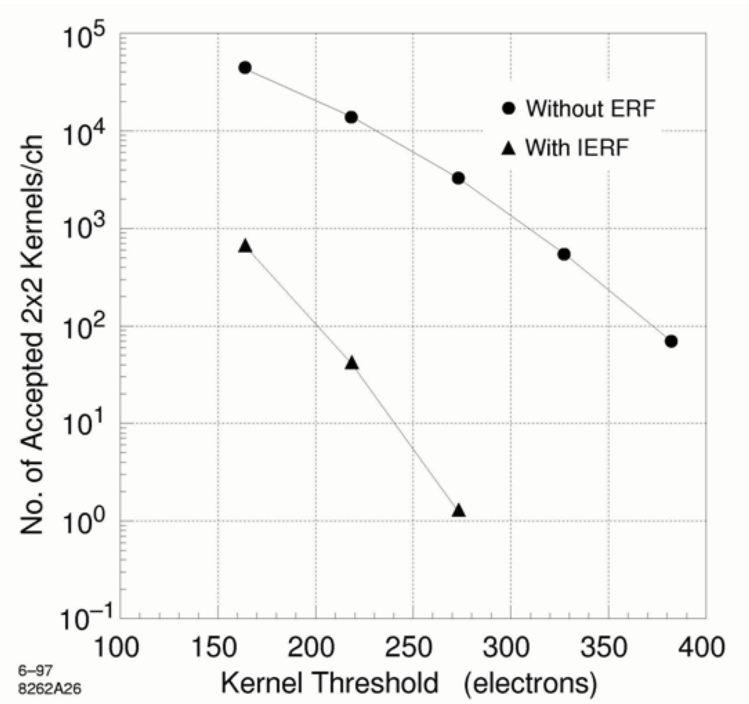
From SLD experience, signal charges stored in buried channel are virtually immune to disturbance by pickup. They were transferred in turn to the output node and sensed as voltages between bunches, when the RF had completely died away

Could this also be done at ILC?

Extended Row Filter (ERF) suppresses residual noise and pickup:



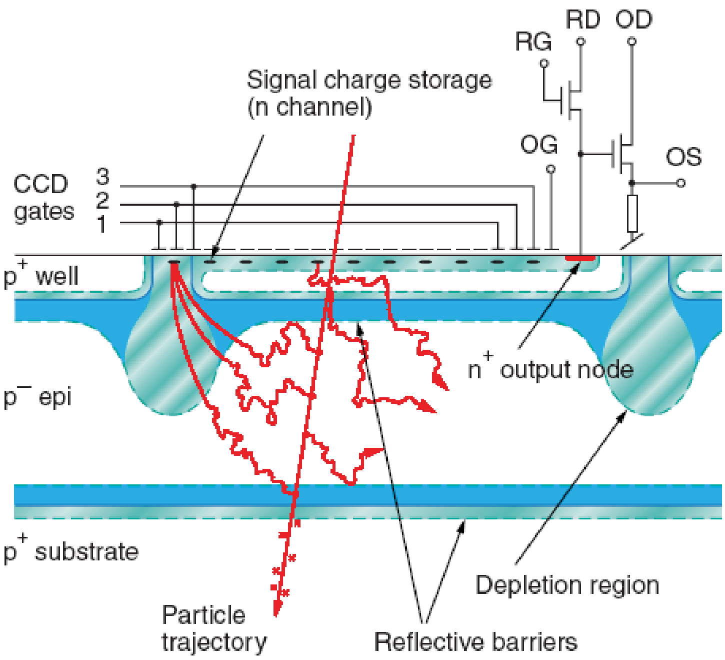
SLD



Without ERF, rate of trigger pixels would have deluged the DAQ system

Read out at 5 MHz, during 'quiet' inter-bunch periods of 8 ms duration

Origin of the pickup spikes? We have no idea, but not surprising given the electronic activity, reading out other detectors, etc



- charge collection to photogate from ~20 μm silicon, mainly by diffusion, as in a conventional CCD
- no problems from Lorentz angle
- signal charge shifted into storage register every 50μs, to provide required time slicing
- string of signal charges is stored during bunch train in a buried channel, avoiding charge-voltage conversion
- totally noise-free storage of signal charge, ready for readout in 200 ms of calm conditions between trains
- 'The literature is littered with failed attempts …'

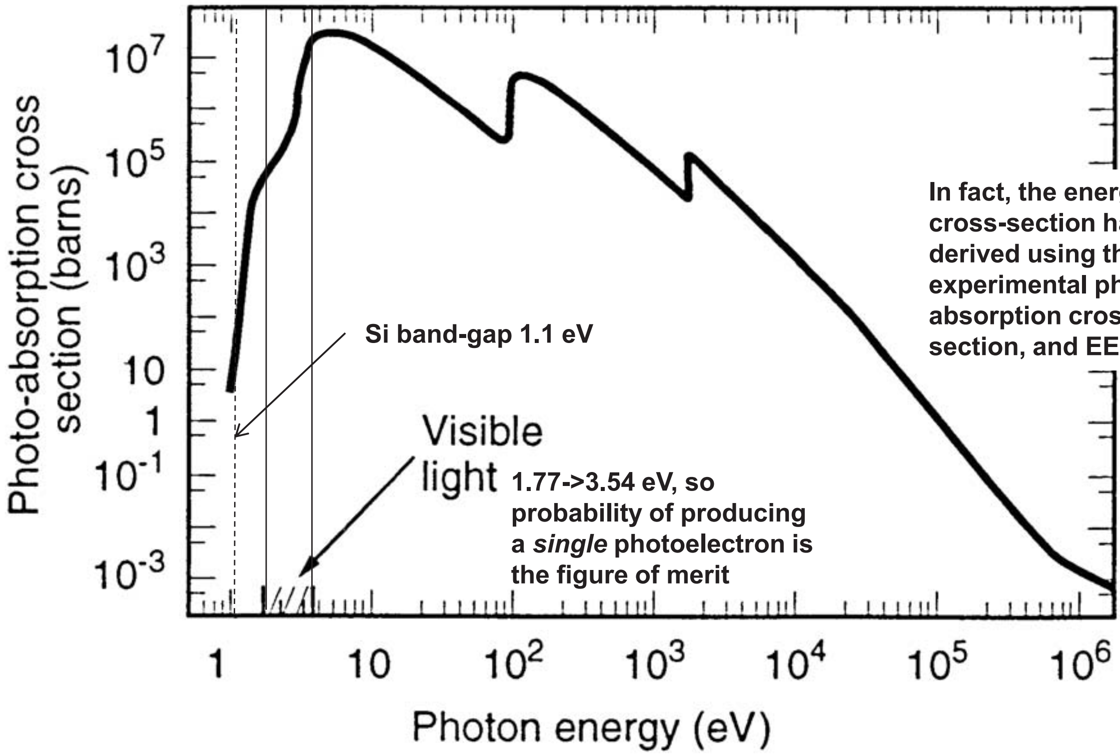
ISIS: Imaging Sensor with In-situ Storage

- Pioneered by W F Kosonocky et al IEEE SSCC 1996, Digest of Technical Papers, p 182
- Current status: T Goji Etoh et al, IEEE ED 50 (2003) 144
- Frame-burst camera operating up to 1 Mfps, seen here cruising along at a mere 100 kfps – dart bursting a balloon
- Evolution from 4500 fps sensor developed in 1991, which became the de facto standard high speed camera (Kodak HS4540 and Photron FASTCAM)
- International ISIS collaboration now considering evolution to 10^7 – 10^8 fps version!

The Founding Fathers – ACCMOR 1980

Missing: Ge Lu, V Ch (taking photo), AG, FW, LL, RE, …

Real photons – closely related!



In fact, the energy-loss cross-section has been derived using this experimental photo-absorption cross-section, and EELS data