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Fine Pixel CCD for ILC Vertex Detector

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FPCCD (Fine Pixel CCD) is developed for the vertex detector at ILC, whose pixel size is $5 \times 5\ \mu\mathrm{m}^2$. The small pixel size of the FPCCD can reduce the hit occupancy below 1% without readout in the intra-train time of ILC. We produced the test-sample of the FPCCD sensor and the prototype of the readout ASIC in 2008. In this paper, the design and performance of them are reported.

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1. Introduction

ILC (International Linear Collider) is planned to construct for the next generation of the high energy frontier physics. In the ILC, electrons and positrons are accelerated along the linear accelerator in an about 30 km long underground straight tunnel [1]. Then, they are collided with each other with the center of mass energy of 500 GeV $-$ 1.0 TeV. One pulse length is about 1 ms, which consists of 2,670 bunches. The beam pulse is repeated at 5 Hz. To obtain high luminosity (2×10^{34} $cm^{-2}s^{-1}$), the beam size is suppressed to σ_x of 639 nm and σ_y of 5.7 nm at the interaction point (IP).

One of the important program at ILC is to study the Higgs mechanism, i.e., measurement of the Higgs coupling to the particle mass. For the particle identification, the flavor tagging of the jets, especially separation of the b-quark and c quark is very important. Therefore, the vertex detector must have good impact parameter resolution of $5 \oplus 10/p\beta \sin^{3/2}\theta$ (μm).

In addition to the position resolution, the hit occupancy is a big problem for the vertex detector at ILC. In the beam crossing, a large number of electron-positron pairs, called pair background, will be generated at IP. The pair background makes many hits in the vertex detector, and the hit occupancy especially at the first layer of the vertex detector becomes large. By the simulation, if all the hits for one beam train are accumulated, it was found that the hit occupancy will become $\sim$10% for the pixel size of 25×25 μm^2. We should suppress the hit occupancy below 1% for the reasonable track reconstruction.

To solve the problem of the hit occupancy, two options are considered. One is to read many times ($\sim$ 20 times) in one train. This option requires the new innovative technology at this moment. The other option is to reduce the pixel size to about 5×5 μm^2. The pixel size of 5×5 μm^2 is already achieved for a CCD (Charge Coupled Devices) camera in a cell phone. Therefore, the latter option could be realized by using CCD technology with relatively low costs. For that reason, we started to develop the FPCCD (Fine Pixel CCD) with the pixel size of 5×5 μm^2 for the vertex detector at ILC [2, 3].

2. FPCCD for ILD Vertex Detector

The FPCCD is a CCD detector whose pixel size is 5×5 μm^2 and thickness of the sensitive layer is 15 μm. Its small pixel size realizes the low hit occupancy below 1% even if the hit signal is accumulated during a total train of 2,670 bunches. The sensitive layer of the FPCCD is fully depleted to suppress the diffusion in the epitaxial layer, and it realizes excellent two-track separation capability. The charges in all the pixels are read in the inter-train time (200 ms), therefore, it is completely free from beam-induced RF noise (EMI). However, since the readout time is relatively long, it will be put in the cryostat of -50 $^\circ$C to reduce the thermal noise.

A schematic design of the FPCCD layer for the vertex detector is shown in Fig. 1. There are two type of the CCD wafers. For the inner most layer, it has 16 readout channels with $128 \times 13{,}000$ pix/ch, and the other has 32 readout channels with $128 \times 20,000$ pix/ch. A horizontal register is prepared between each readout channel to transfer the signal charge to the output node, whose size is the same as the readout pixels (5×5 μm^2). The pixels in it are also sensitive to the charged particles. The horizontal transfer has larger number of pixels than the vertical transfer. Since charge

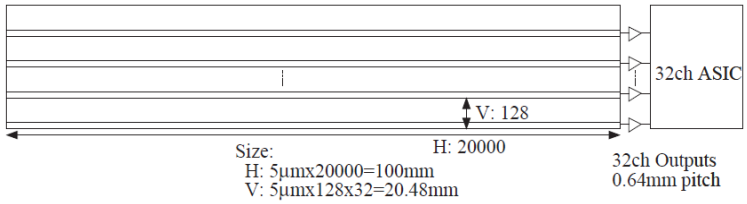

Figure 1: A schematic view of the FPCCD ladder.

	wafer size (mm^2)	ch/wafer	No. of wafers	No. of readout channels
L1a	10.24 x 65	16	15(ϕ) $\times$ 2 (Z)	480
L1b	10.24 x 65	16	15(ϕ) $\times$ 2 (Z)	480
L2a	20.48 x 100	32	16(ϕ) $\times$ 2 (Z)	1,024
L2b	20.48 x 100	32	16(ϕ) $\times$ 2 (Z)	1,024
L3a	20.48 x 100	32	16(ϕ) $\times$ 2 (Z)	1,536
L3b	20.48 x 100	32	16(ϕ) $\times$ 2 (Z)	1,536
Total			220	6,080

Table 1: The number of the CCD wafers and readout channels for the FPCCD vertex detector. L1 $\sim$ 3a and L1 $\sim$ 3b are placed on both sides of a plate structure and consist of the layers of the sensor ladder.

in the vertical register is transferred to the horizontal register after charge in all the horizontal register is readout, the horizontal transfer has higher transfer rate than the vertical transfer. This configuration is, therefore, more advantageous to reduce the dark current induced by the irradiation. The CCD wafer and ASICs are placed on both sides of a plate structure of about 2 mm thickness which is made of a low-mass material like rigid foam. Then, three layers of the sensor ladder will be located around the IP as the vertex detector. The number of the CCD wafers and readout channels for the FPCCD vertex detector is summarized in Table 1.

There are some requirements to the FPCCD vertex detector at ILC. Because of small pixel size of the FPCCD, there are a large number of pixels in one channel (20,000 x 128). Therefore, the readout speed must be above 10 Mpix/sec to read all the pixels in the inter-train time. If a particle penetrates a pixel horizontally, the path length in a pixel becomes small due to the small pixel size. In that case, the signal level will be only 500 electrons. Therefore, the total noise level below 50 electrons is desirable. The vertex detector will be located in a cryostat, and the power consumption in a cryostat is required to be below 100 W. Since there are about 6,000 channels in the FPCCD vertex detector, the power consumption below 16 mW/ch is required to each channel. To achieve these requirements, development of the FPCCD sensor and readout ASIC was started.

3. FPCCD test-sample

Test-samples of the FPCCD was developed by Hamamatsu [4] in 2008 as shown in Fig. 2. The purposes of the FPCCD test-sample is to realize the readout speed of 10 Mpix/s, the noise level below 50 electrons, and the power consumption below 10 mW/ch. The chip size is 8.2 $\times$ 7.5 mm^2 and there are 4 readout channels which contain 512 $\times$ 128 pixels. Although the final goal of

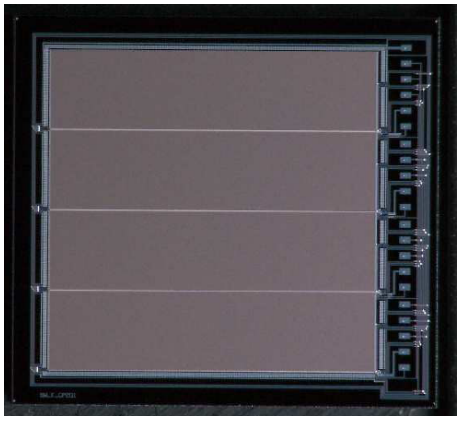

Figure 2: A picture of the FPCCD test-sample.

the pixel size is 5×5 μm^2, that of the test-sample is 12×12 μm^2. The horizontal transfer register could be prepared between each readout channel whose size is the same as the readout pixels (12×12 μm^2). In this production, we produced the test-sample with two kinds of the epitaxial layer thickness, 15 μm and 24 μm. Since the epitaxial layer of 24 μm thickness has higher resistivity, it is easier to be fully depleted than that of 15 μm thickness. The amplifier block consists of three stages of the source follower circuits with a load resistor of 10 kΩ. We prepared 7 variants of the amplifier block, which are different in combination of the drain current.

The output signals were checked at the readout speed of 10 Mpix/s by Hamamatsu as shown in Fig. 3. The clear rectangle shape of the signal output can be observed for the drain current of 1.57 mA/amp (Fig. 3(a)), where mA/amp means the total current at the amplifier block. In this case, the power consumption at the amplifier block is 15.7 mW/amp. Since low drain current is important to realize the low power consumption, the output signal was checked for lower drain current. Fig. 3(b) shows the output signal for the drain current of 1.14 mA/amp, where the power consumption at the amplifier block is 11.4 mW/amp. As shown in Fig. 3(b), the rise and fall time constant becomes large for low drain current in the amplifier. Even in the case of 1.14 mA/amp, we can readout the output signal because the rise time is within a half of the readout cycle. The optimization of the drain current and the amplifier design must be investigated.

There are some issues to be improved for the future production of the test-sample. Figure 4 shows the output charge from the test-sample along the horizontal layer for the epitaxial layer thickness of 15 μm. The dark current becomes large at the horizontal edge. In addition, the output charge is fluctuated for each vertical line, depending on the charge transfer efficiency. Both problems come from the design of the layout and the solution is already devised. Since the fluctuation of the output charge for each vertical line can be recovered by minor modification of the layout, it will be fixed for the next production in 2009.

4. Readout ASIC for FPCCD

Together with the FPCCD sensor itself, development of the readout ASIC is important issue. There are some requirements to the readout ASIC due to characteristics of the FPCCD as shown

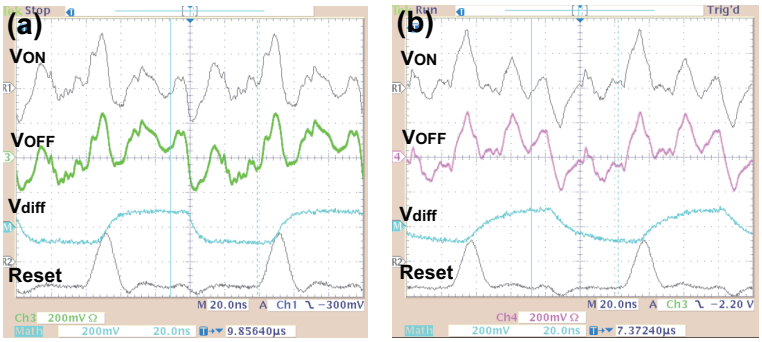

Figure 3: The output signals measured by FET probes for the drain current in the amplifier of 1.57 mA/amp (a) and 1.14 mA/amp (b), where the thickness of the epitaxial layer is 15 μm. The power consumption at the amplifier block is 15.7 mW/amp and 11.4 mW/amp for 1.57 mA/amp and 1.14 mA/amp, respectively. In the figures, V_{ON} and V_{OFF} are the output with and without light illumination, and $V_{diff} = V_{OFF} - V_{ON}$.

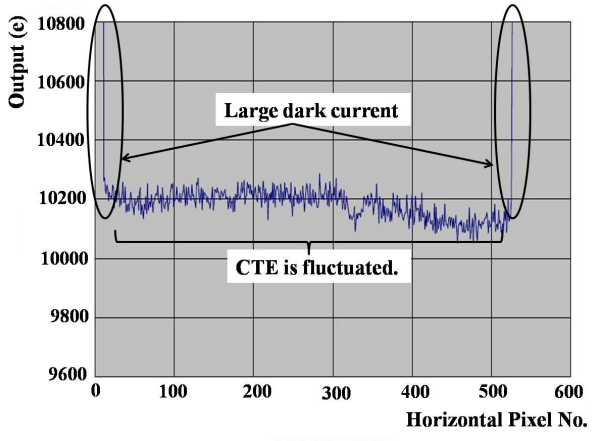

Figure 4: The output charges along the horizontal layer for the epitaxial layer thickness of 15 μm. The dark current becomes large at the horizontal edge. In addition, the output charges are fluctuated for each vertical line, depending on the charge transfer efficiency (CTE).

in Section 2. At first, the readout speed must be above 10 Mpix/sec to read all the pixels in the inter-train time. Since the noise level is required to be below 50 electrons in total, the goal of the noise level in the readout ASIC was set to below 30 electrons. The power consumption must be below 16 mW/ch due to cooling power of the cryostat and the FPCCD sensor will consume about 10 mW/ch. Therefore, the power consumption at the readout ASIC must be below 6 mW/ch. To achieve these requirements, the design of the readout ASIC was determined.

The readout ASIC was designed to have an amplifier, low-pass filter (LPF), correlated double sampling (CDS), and two charge sharing ADCs (Analog to Digital Convertors) [5] as shown in Fig. 5. The readout with 10 Mpix/sec will be achieved by using two charge sharing ADCs alternatively, where the readout speed of one ADC is 5 Mpix/sec. The noise level will be reduced to 30 electrons by LPF and CDS. The charge sharing ADC uses successive approximation technique for A/D conversion, comparing the charges stored in the capacitors. Since this technique can reduce the

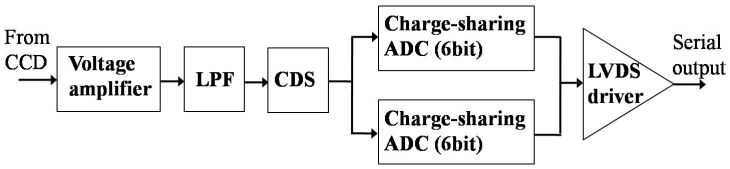

Figure 5: A schematic diagram of the circuit blocks in each channel of the readout ASIC.

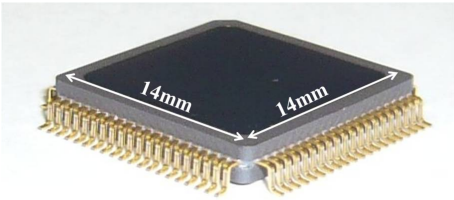

Figure 6: A picture of the readout ASIC with QFP-80 package.

current in the circuit much smaller, low power consumption below 10 μW can be realized at the ADC block. We confirmed that the readout ASIC satisfies the requirements to the readout speed and noise level by the SPICE simulation. A prototype of the readout ASIC was produced in 2008 with 0.35 μm TSMC process as shown in Fig. 6. The chip size is 2.85 $\times$ 2.85 mm^2, where 8 readout channels are prepared. The readout ASIC is packaged with QFP-80 for the response test.

To check the readout ASIC, the test system was constructed based on the VME system. A GNV-250 module was used for the operation and data readout, which was developed as the KEK-VME 6U module. Two daughter boards for TTL input/output and LVDS input were attached on the module. The readout ASIC was put on the test-board, and connected to the GNV-250 module. Since a FPGA is equipped on the GNV-250 module, any logic can be realized by changing the program implemented into a FPGA. The ADC information read from the readout ASIC are stored in FIFO prepared at the FPGA, then, it is sent to a computer.

At first, the response of the circuit elements in the readout ASIC was checked. The internal signals after the pre-amplifier and before ADCs can be checked by using the monitor output prepared at those position, and they were observed as expected by the SPICE simulation. Then, output signals from ADCs were investigated. We could observe the serial output from ADCs, synchronizing with the operation signals as shown in Fig. 7. We, therefore, readout the ADC information by a computer and studied performance of the readout ASIC.

As the first step of the performance study, the noise level in the ASIC was investigated. Figure 8 shows the pedestal distribution. We found that some ADC counts are not output from the ADC due to the precision of the capacitance for the MSB (Maximum Sensitive Bit). The r.m.s. of the pedestal distribution is 1.0 ADC count and this fluctuation is partially attributed to the lost ADC numbers. The equivalent noise charges were evaluated as 40 electrons (r.m.s.), where 5 μV/e is assumed as the FPCCD output and 0.2 mV/ADC are used as the ratio of the FPCCD output to ADC count. Since the requirement to the noise level is below 30 electrons, this result is almost acceptable. The precision of the MSB capacitor can be improved by dividing it to small

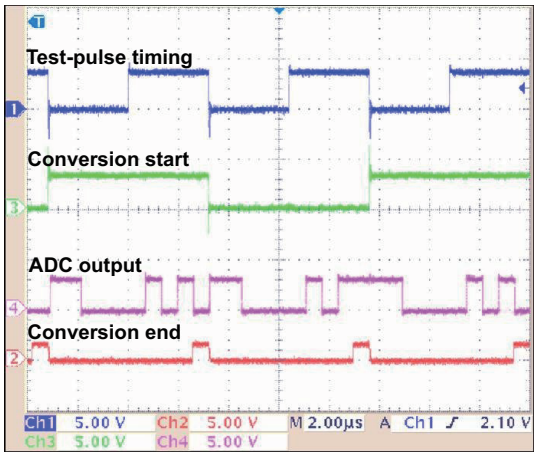

Figure 7: The output signals from the ADC in the readout ASIC. The serial output from ADC was obtained.

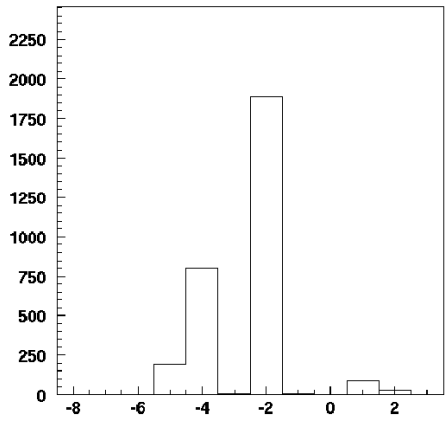

Figure 8: The pedestal distribution obtained for one ADC. There is no events at -3 ADC counts due to the precision of the capacitance for the MSB in the ADC.

capacitance. Therefore, the noise level will be smaller for the next production.

For the next step, the ADC linearity to the input voltage was studied. Figure 9 (a) shows the equivalent charges in the FPCCD sensor evaluated by the ADC output as a function of the input voltage of the test-pulse. Fitting this plot with a linear function, deviation of the equivalent charges from the linear fitting was obtained as shown in Fig. 9 (b). From this result, the ADC linearity within $\pm$60 electrons was derived, where this fluctuation partially comes from the lost ADC numbers.

The amplifier gain can be adjusted from 2 to 16 by sending signals for the parameter setting to the gain adjustment block. We checked accuracy of the gain adjustment. The ADC output was obtained as a function of the amplifier gain, and it was fitted by a linear function. The deviation of ADC values from the linear fitting was within $\pm$5%. Therefore, we confirmed that the amplifier gain can be adjusted within $\pm$5% accuracy. Since the fluctuation of the gain adjustment comes from the lost ADC counts, this linearity will be improved after modification of the MSB capacitors

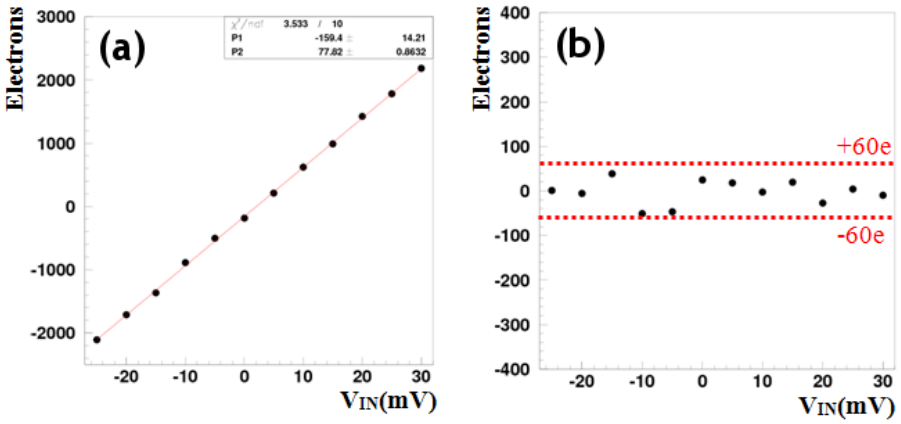

Figure 9: (a) Equivalent charges in the FPCCD evaluated by ADC output as a function of the input voltage of the test-pulse (V_{IN}). (b) The deviation of the equivalent charges in the FPCCD from the linear fitting of (a) as a function of the input voltage of the test-pulse. The linearity is within $\pm$60 electrons.

in the ADCs.

5. Summary

We develop the vertex detector for ILC using the FPCCD. The test-sample of the FPCCD was developed by Hamamatsu. The output signal can be observed from the test-sample with the readout speed of 10 MHz/pix. The rise and fall time constant becomes large for low drain current in the amplifier. The optimization of the drain current and the amplifier design must be investigated. Large dark current at the horizontal edge and fluctuation of the output charges in each vertical layer come from the design of the layout. The latter problem will be recovered by minor modification of the layout for the next production in 2009.

In addition to the FPCCD sensor, the readout ASIC was also developed. All the circuit blocks were confirmed to work correctly. We found that some ADC counts are not output from ADCs due to the precision of the capacitance for the MSB. At this condition, the equivalent noise charges in FPCCD was 40 electrons and this result was almost acceptable. The ADC linearity to the input voltage was within $\pm$60 electrons. The noise level and ADC linearity will be improved after modification of the MSB capacitors in the ADCs.

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