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SLHC tracker upgrade: challenges and strategies in ATLAS

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The Large Hadron Collider (LHC) will be upgraded to the Super-LHC in ≈2016 to provide a ten-fold increased luminosity and data rate. The inner silicon tracking detectors of the ATLAS and CMS experiments will be replaced by even more powerful devices. The new detectors will face unprecedented particle densities and radiation levels. Limiting the power consumption of the front-end electronics, distributing power efficiently and minimizing detector mass, while keeping the costs of the detector affordable, are key challenges. Possible design solutions and the status of R&D for ATLAS are described.

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1. Introduction

The Super-LHC (SLHC) is the upgrade of the Large Hadron Collider (LHC) by ≈2016 to deliver a ten-fold increased luminosity. The SLHC has been recognized as the highest priority project for particle physics in the European Strategy roadmap approved by CERN Council in 2006 [1]. The anticipated costs for the accelerator upgrade are ≈1 B€. Assuming that the LHC experiments have delivered major scientific discoveries by 2015 already, why should the LHC be upgraded? Without knowing the exact nature of the anticipated LHC discoveries three generic physics reasons for the SLHC can be given:

- Consolidation of the LHC discoveries (e.g. Higgs boson, Supersymmetry, Z' or other)
- Extended discovery reach by ≈30% in mass or ≈1 TeV for direct searches (e.g. heavy scalar quarks or gluinos)
- Increased precision and access to rare decays/channels (e.g. flavor-changing top decays, triple Higgs boson coupling, multi-gauge boson production)

Details have been worked out for specific physics scenarios [2]. Other relevant considerations strongly in favor of the SLHC upgrade are:

- Hadron colliders can be competitive for several decades (e.g. Tevatron)
- No other affordable new accelerator could cover or extend the SLHC effective energy range
- The electron positron linear collider ILC might be delayed
- The SLHC assures continued European leadership in particle physics

The LHC inner detectors will suffer severe radiation damage and need to be upgraded to cope with the increased occupancies and radiation levels of the SLHC. Strategies and possible solutions are described for the ATLAS inner tracker upgrade. The focus is on silicon strip, not pixel, detectors.

2. Challenges, specifications and constraints

Lacking operational experience of the LHC, the SLHC beam parameters are not well known and will probably remain uncertain for several years to come. The heating up of the vacuum chamber through the electron cloud effect [3] in combination with limited vacuum chamber cooling capacity seem to rule out an increase of the beam collision rate. The luminosity increase has thus to be achieved by packing more protons into each bunch and by stronger focusing at the collision point. The parameters of two alternative scenarios are listed in Table 1 together with the design LHC parameters. Both upgrade scenarios are very challenging

for the new tracker since the number of overlap events is enhanced from ≈19 at the LHC to 300-400 at the SLHC.

	SLHC		LHC
Bunch spacing [ns]	25	50	25
RMS bunch length [cm]	7.55	11.8	7.55
Luminous region [cm]	3.7	5.3	4.5
Peak luminosity [10^{34} cm^{-2} s^{-1}]	15.5	10.7	1
Overlap events	296	403	19
Initial luminosity life time [h]	2.2	4.5	22
Effective luminosity [10^{34} cm^{-2} s^{-1}] (5h turn-around)	3.6	3.5	0.56

Table 1: Machine parameters for two SLHC scenarios and the LHC (nominal) [3]

There are other more technically trivial, but very relevant constraints: limited time, money and effort will be available for R&D of the SLHC trackers, since commissioning, operation and exploitation of the LHC is the highest priority. The new tracker has to fit in the existing detector volume and be compatible with some of the existing infrastructure. Shut-down and installation periods must be minimized for many reasons. The time scale for compiling a Technical Design Report (TDR) for the ATLAS Detector Upgrade is beginning 2010.

Despite many uncertainties the basic features of the new tracker can be derived from simple assumptions once a few crucial parameters like the anticipated increase in luminosity and the number of overlap events are fixed. This is illustrated in Figure 1.

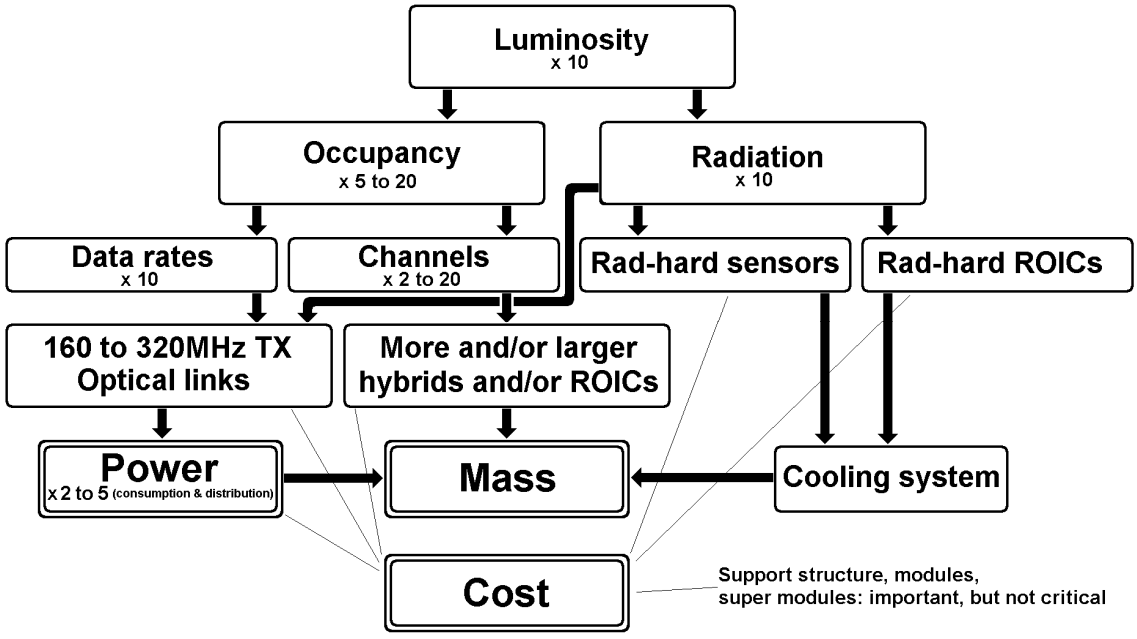

Figure 1: Challenges of the SLHC trackers. The numbers indicate the increase in luminosity, occupancy, radiation levels, etc. compared with the LHC. See the text for further explanations.

The increased luminosity leads to increased radiation doses, particle fluences and occupancies (fraction of channels per collision hit by a particle). The radiation dose is proportional to luminosity[1] while occupancy depends on the collision rate as well. The extreme radiation levels at the SLHC lead to a number of specific design challenges for read-out integrated circuits (ROIC), silicon sensors and optical signal transmission, which we believe will be met. The impact of radiation on the overall design is limited and mostly affects the cooling system, which has to provide reduced sensor temperatures to minimize sensor leakage currents.

The increased occupancy, in contrast, has a huge impact and effectively shapes the new tracker. The larger number and density of electronics channels lead to increased power consumption, more and/or larger hybrids carrying more ROICs, naively requiring more cables and increasing detector mass. Power consumption, power distribution and detector mass are the critical areas that demand innovative solutions to make tracking at SLHC possible. Figures 2 and 3 illustrate the concentration of cables leaving the current ATLAS inner tracker and the total material the tracker represents. The figures clearly suggest that cable congestion and detector mass have reached a deplorable scale and must not grow in future detectors.

Figure 2: End view of the ATLAS barrel detector. The cylindrical SCT is placed in the centre of the detector at a radius of 25 cm to 55 cm from the beam line. The (red) cable strands extending from the centre to larger radii at 2, 4, 8 and 10 o'clock are the SCT power cables. The same number of cables leaves the other end of the detector.

[1] Note that this is a genuine LHC and SLHC feature. Radiation is dominated by machine background and beam losses at other colliders.

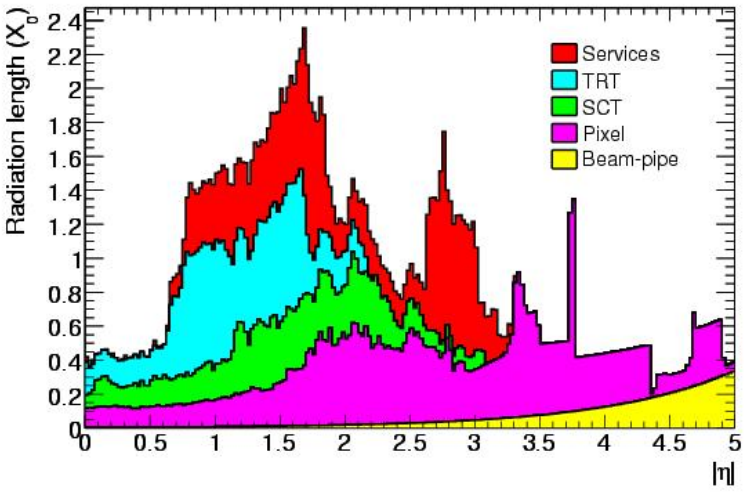

Figure 3: Material represented by the ATLAS inner tracker (Pixel, SCT and TRT) in radiation lengths as a function of pseudo rapidity.

3. Power consumption, power distribution and cooling

The ATLAS silicon trackers consume many tens of kW of power[2], dominated by the read-out electronics [4]. The power consumption per channel is likely to decrease at the SLHC mostly due to the reduced operation voltage of the future ROICs. The targeted reduction to ≈ 1.6 mW per strip and ≈ 50 μW per pixel is however insufficient to compensate for the larger number of channels of the new trackers. Reducing the "current consumption" is significantly harder than reducing power due to enhanced functionality, higher data rates and increased sub-threshold leakage currents. It is thus prudent to assume total power will at least triple and total current will at least increase by a factor of five compared with the LHC silicon trackers.

The increased power combined with the requirement for reduced sensor temperatures and the increased current lead to tight requirements for the cooling system. The experience with cooling systems for the LHC detectors, in tracking and elsewhere, has at best been mixed. Different cooling pipes and coolants have been chosen. Aluminum pipes are e.g. implemented in the ATLAS pixel detectors while copper-nickel pipes are used for the SCT. The ATLAS trackers use evaporative cooling while CMS does not. The common difficulty is finding the right balance between minimum mass, cooling performance and robustness.

While evaporative cooling is not without practical difficulties, it seems to be suited best for the SLHC inner trackers and is the only solution considered by ATLAS. The main coolant candidates are C_3F_8 (as used for the current ATLAS tracker) and CO_2 (as used by LHCb). These are rather orthogonal alternatives with CO_2 requiring feed pressures of ≈100 bars and

[2] The total rack power supply including optical links and cable losses, but excluding silicon sensors, is 30 kW for the ATLAS pixel and 45 kW for the SCT.

correspondingly robust pipe work. An R&D program on pipe materials and joining and welding techniques has started. One aim is to use commercial solutions wherever possible. The choice of coolant will also have significant impact on module and supermodule design. The cooling capacity of C_3F_8 is limited and makes achieving a small temperature drop of a few degrees between coolant and silicon sensor more important than for a CO_2 system.

Power distribution has been recognized as a possible show-stopper for the SLHC trackers and an intense R&D effort is devoted to solving it. Independent powering with one set of cables for each module fails for several reasons including: lack of space to feed additional power cables to the trackers, increased mass and reduced power efficiency. The latter is important because thermal losses present an additional load to the cooling system. The power efficiency of the LHC trackers is already fairly low and ranges between 20% (pixels) to 50% (strips); at SLHC it could easily drop to 10% or less.

The increased module current at SLHC is the underlying cause of the power distribution challenge and consequently delivering module power at reduced current provides a solution. The two fundamentally different approaches investigated in ATLAS are a) serial powering and b) power transmission at high DC-DC voltage and low currents combined with local DC-DC conversion. Both concepts are promising and if power distribution R&D continues to be successful, the familiar picture of particle detectors congested by power cables will belong to the past. A comprehensive description of this R&D is given in these proceedings [5] and elsewhere [4].

4. Electronic components

The R&D of the ATLAS SLHC silicon tracker has gained a lot of momentum in the recent three years and first prototypes of application specific electronic components are being designed. Below I will discuss some of their generic features and focus on silicon strip sensors.

4.1 Sensors

Silicon sensors placed at a radial distance of ≈30 cm from the SLHC beam line have to withstand an equivalent fluence of $\approx 10^{15}$ 1-MeV neutrons/cm^2. Conventional p-doped strips on n-bulk silicon as used for the SCT are not suitable for this task, but n-on-p sensors are expected to be fine.[3] Recent R&D on radiation-hard silicon sensors is described in [6]. The need to operate sensors at ten-fold increased radiation levels and the choice of n-on-p sensors affects the overall detector system in three ways.

- The sensors need to be cooled to ≈-25 °C rather than to ≈-7 °C as for the ATLAS SCT to limit leakage current in order to avoid thermal run-away and increased shot noise. The increase in leakage current is due to radiation damage in the silicon substrate

[3] N-on-p sensors are cheaper than n-on-n sensors as used for the ATLAS pixels and elsewhere since the backside of the sensors does not need to be processed, which leads to ≈60% cost reduction.

crystal lattice. Damage does not depend on the details of the sensors and operation at low temperature is the only way to deal with it.

The tightened temperature requirement has a major impact on the cooling system and module design.

- The sensor bias voltage will increase to values of 500 V to 800 V or even higher to minimize charge trapping and enable a minimum signal of ≈15,000 electrons in 300 μm thick silicon sensors. These bias voltages require high-quality silicon sensors and constrain cable ratings. The latter is important if the cables installed for the LHC trackers were to be reused at SLHC.

- The signal polarity is changing since electrons rather than holes are collected. This requires a modified preamplifier circuit. The reduced signal requires a low-noise preamplifier and comparator to enable operation at reduced comparator thresholds (for a binary read-out chip architecture).

A parameter that is arguably much more relevant then sensor temperature, bias voltage or signal polarity is *sensor area*. Maximizing sensor size reduces the number of components (sensors, hybrids, modules, etc.) of a tracking detector and could significantly simplify production and assembly. ATLAS has chosen 100 mm x 100 mm sensors as the baseline for their new silicon strip tracker. This corresponds to the maximum useful silicon area that can be cut out of a 150 mm diameter wafer.

While sensor area is to some degree a matter of choice, the length and pitch of silicon strips are constraint by occupancy and required space resolution. The baseline value adopted by ATLAS for the inner detector region has a pitch of 75.6 μm and a strip length of 2.5 cm (see Figure 4).

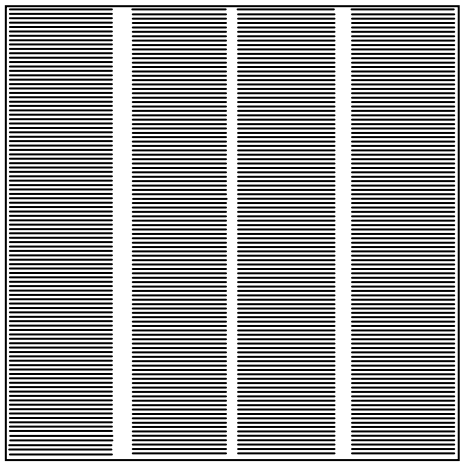

Figure 4: A short strip sensors for SLHC tracking with four columns of 2.5 cm long strips on a 100 mm x 100 mm sensor. The strip pitch is not to scale.

4.2 Hybrids

The hybrids (multi-chip modules) carry the read-out integrated circuits and various passive components; receive and distribute power, clock and command signals; send out the data

stream; provide a low thermal impedance path to the cooling pipes; etc. The increased track density and channel number at the SLHC aggravates a number of traditional challenges for hybrid design.

- There will be either more, longer or wider hybrids compared with the LHC trackers, which increases detector mass.
- Despite power savings per channel, total hybrid power is expected to increase. This poses a challenge to the local power supplies on the hybrid and complicates thermal management.
- Finally, the increased data bandwidth requires to either route more data lines off the hybrid or preferably to operate at higher data and clock frequencies which makes suppression of cross-talk and "pick-up" more critical than at LHC.

Figure 5 shows a comparison between the SCT hybrid and a possible successor for SLHC short-strip sensors. The SCT hybrid [6,7] is a Polyimide-copper flexible circuit with a row of twelve ABCD chips and a commercial connector at its end. The flexible circuit is reinforced by a 0.3 mm thick carbon-carbon substrate which serves as a mechanical support and thermal path. The hybrid is separated from the sensor by a ≈1 mm thin air gap. The hybrid wraps around the SCT module and thus serves both the top and the bottom sensor.

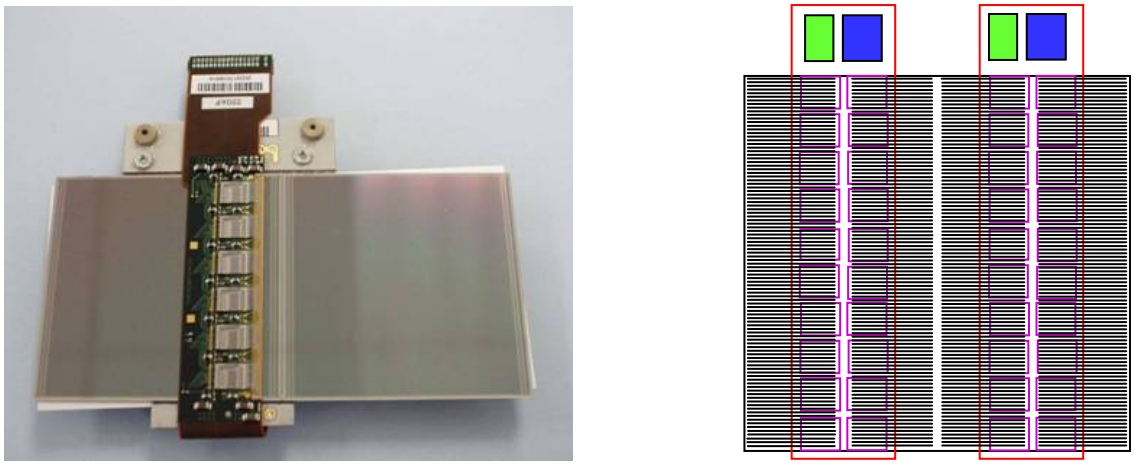

Figure 5: (Left) Photograph of an SCT module. Only the top side of the 12-chip hybrid is visible. The module top sensor and back sensor are titled by 40 mrad. (Right) Sketch of two SLHC short-strip module hybrids. In this layout each hybrid carries twenty ROICs, a local power supply chip and a module controller/slow-control chip. Connectors are not shown.

The design of the SLHC hybrid is still in its infancy. A typical arrangement is shown in Figure 5. Rather than having four hybrids, each serving a column of strips, two hybrids with a double row of chips are used. Fan-outs are avoided, assuming that high-yield wire-bonding at an angle is possible with modern bonding machines. The gaps between adjacent ROICs enable decoupling capacitors for analog power to be placed close to the chips. The hybrid would carry a local power supply and data multiplexer, decoder and slow-control chip at it end. Such a design would typically be 110 mm long and 20-25 cm wide, depending on readout chip width. The structure of the sensor with columns of strips implies that the hybrid will have to be placed above the sensor (rather than next to it) in order to connect to each strip.

Hybrid mass would increase from ≈0.4% of a radiation length (averaged over sensor area) to at least twice this value but possibly significantly more. This makes the hybrid one of the most massive module components. It is important to innovate in order to reduce hybrid mass further. Gluing the hybrid directly to the sensor as advocated in [9] is one approach which would also simplify thermal management. R&D is being started to evaluate the long-term risk of creating surface charges or diffusion of impurities in connection with radiation.

One particular innovative approach is "3D packaging" of sensors and different layers of electronic circuits, connected through vertical interconnects [10]. The 3D stacks can be built using wafer-to-wafer or die-to-wafer bonding with the technology of each layer being optimized for its function. While this approach is not likely to be practical at the time scale of the SLHC, *post-processing of silicon sensors* is an interesting "poor man's" alternative.

In the latter approach thin-film dielectric and metal layers would be deposited to the sensor wafer to build up the hybrid circuitry. The ROICs could be wire-bonded or bumped on the top metal layer. Using thin-film technology helps to reduce area and thickness of the "hybrid" significantly. (First estimates suggest a reduction of a factor two to three compared with Polyimide-copper flexible circuits.) The thermal properties of a module built in this technology are expected to be excellent. The electrical performance of post-processed hybrids is not understood. The consequences of increased strip capacitance due to the proximity of hybrid metal layers to the sensor and the reduced thickness of metal layers need to be studied. Other unknowns are yield and costs. Thin-film hybrids have, to the best of our knowledge, not yet been implemented in particle physics instrumentation, but were prototyped successfully during ATLAS pixel module development [11].

4.3 Read-out integrated circuits

The ROIC of the SCT, the ABCD chip [12], is produced in a radiation-hard DMILL 0.8 μm bi-CMOS technology. The target technology for the ROIC, called ABC-Next, to readout the ATLAS silicon strip tracker for SLHC is 0.13 μm CMOS. As a power saving alternative, 0.13 μm SiGe (strained silicon) processes are investigated as well [13].

ATLAS have chosen a two-step strategy to develop the new ROIC. First a 0.25 μm CMOS version of the ABC-Next will be produced. The design is well advanced and a submission is scheduled for spring 2008. In a second step, the 0.13 μm CMOS version will be designed. Breaking down the project in this way allows us to get a functional and affordable chip (in 0.25 μm CMOS) for prototyping of silicon modules and supermodules on a short time scale. The design of the much more expensive 0.13 μm CMOS version can then be based on mature specifications and focus on technology challenges.

The ABC-Next specifications are much enhanced over the ABCD: data can be readout-out at 40, 80 or 160 MHz rather than at 40 MHz; the chip contains various power management features including shunt regulators and transistors to enable serial powering and linear regulators to provide analog voltage; the front-end can accept input signals of both polarities; pipeline depth is increased; the chip ID field is increased to address the large number of chips on a supermodule; LVDS data drive currents can be adjusted; etc.

At this stage the ABC-Next has 128 channels. In the future we will consider enlarging die area and channel number, which could result in overall power and real estate savings and again reduce the number of components.

5. Overall layout

The overall layout of the future ATLAS tracker is not well understood at this early stage and the number, position and required space resolution of the detector layers need to be optimized further using detailed simulations. Two representative arrangements are shown in Figure 6. The tracker is expected to be an all silicon tracker with three (or four) pixel layers near the beam pipe and outer strip layers. The geometrical acceptance extends to $-2.5 < \eta < 2.5$ and a barrel and disk region. The number of space points in both arrangements is relatively low (5 strips and 3-4 pixel hits). Many details will influence the detector layout but experience from LHC tracker construction suggests that the layout will most of be determined by services (electrical, cooling and optical). Understanding and minimizing the service volume, optimizing the service path through the inner tracker and finding the best position for feed-throughs and connectors will be crucial.

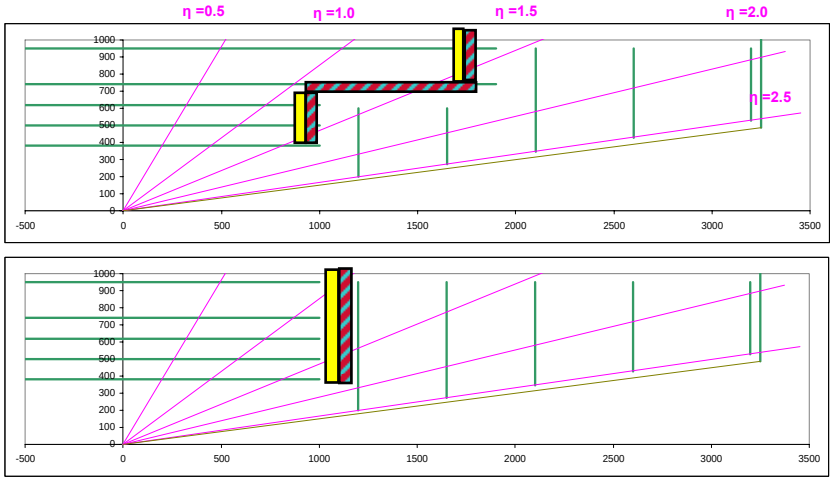

Figure 6: Possible layer arrangement of the ATLAS SLHC tracker in an r-z view. Only one quadrant of strip layers is shown. The inner pixel layers are omitted. Dimensions are in mm. The pink lines indicate pseudo rapidity. The colored squares at the end of the barrel indicate connector positions and service routing. (Top) Layout with two long outer barrel layers. (Bottom) Layout with a fixed-length barrel.

6. Conclusions

The LHC luminosity upgrade and the replacement of the ATLAS and CMS inner trackers will ensure that the LHC physics potential is fully exploited. The new trackers will be the largest and most complex silicon detectors ever built and will have an unprecedented number of electronic channels. The key challenges relate to power distribution, thermal management and detector mass. Many innovative concepts to overcome these difficulties have been identified. The next few years of R&D will show if these detectors can be built in time, at an affordable cost and with the desired performance.

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