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Readout Electronics for the ALICE Time Projection Chamber

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In this paper we present the architecture of the Readout Electronics for the Time Projection Chamber (TPC) of the ALICE experiment at CERN LHC. The ALICE TPC electronics consists of 557568 channels. A single readout channel is made of two basic units: (a) an analogue ASIC (PASA) that incorporates the shaping/amplifier circuits for 16 channels; (b) a mixed-signal ASIC (ALTRO) that integrates 16 channels, each consisting of a 10-bit 25-MSPS ADC, the baseline subtraction, tail cancellation filter, zero suppression and multi-event buffer. The complete readout chain is contained in Front End Cards (FECs), with 128 channels each, connected to the detector by means of kapton cables. From the control and readout point of view the FECs are organized in 216 partitions, each being an independent system steered by one Readout Control Unit (RCU). The RCU, which is physically part of the on-detector electronics, implements the interface to the Data Acquisition (DAQ), the Trigger and Timing Circuit (TTC) and the Detector Control System (DCS). It broadcasts the trigger and clock information to the FECs, performs the initialization and readout via a high bandwidth bus, and implements monitoring and safety control functions via a dedicated link. The radiation load on the TPC is low (1 krad $\oplus$ 10^{11} neutrons/cm^2 over 10 years). Thus standard radiation-soft technologies are employed for the implementation of this electronics. However, some special care has been required to protect the system against potential damages caused by Single Event Effects. A fraction of the final electronics has been benchmarked by realistic measurements with a prototype of the ALICE TPC. Test show that the system fulfils all design requirements. At present, the mass production of all components is being completed. After the installation of the electronics, the whole detector will undergo a six month commissioning phase before being lowered into the experimental hall in fall 2006.

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1. Introduction

The ALICE Time Projection Chamber (TPC) [1] consists of a cylindrical gas volume (about 90 m^3 of Ne-CO_2-N_2), divided in two drift regions by a high voltage plane located at its axial centre, under a uniform electrostatic field. At the endplates, conventional Multi-Wire Proportional Chambers (MWPC) provide a charge amplification and readout by means of a cathode plane segmented in about 560000 pads. The signal released is characterised by a fast rise time (less than 1 ns) and a complex long tail. This tail, causing pile-up effects, sets the main limitation to the maximum track density at which a MWPC can be operated. Therefore, an accurate tail cancellation and baseline restoration of the detector signals are some of the very demanding specifications implemented in the readout electronics, together with the possibility of performing on-line data compression.

The TPC will be operated at a maximum trigger rate of 200 Hz in Pb-Pb running and 1 kHz in p-p running, producing respectively 142 GByte/s and 710 GByte/s of uncompressed data, with a signal occupancy in the innermost chamber up to 50%.

2. System Architecture

The readout of the ALICE TPC is organized in 216 partitions equipped with a different number of Front End Cards (FEC) [2] connected to the detector pad-plane by means of kapton cables. Every FEC (fig. 1) integrates the electronics to process 128 pad signals and it consists of the following basic units: 8 analogue ASICs (PASA), each one incorporating a charge sensitive amplifier and a semi-Gaussian pulse shaper of the 4^{th} order for 16 channels; and 8 mixed-signal ASICs (ALTRO) [3], each integrating a 10-bit 25-MSPS ADC, a very sophisticate processing chain, performing the baseline subtraction, tail cancellation and zero-suppression, and a multi-event buffer for 16 channels. Data from the ALTRO can be read out at a maximum speed of 60MHz through a 40-bit wide bus, yielding a total bandwidth of 300 Mbyte/s. Moreover, the readout speed and the ADC sampling frequency are independent. Therefore, the readout frequency does not depend on the bandwidth of the input signal being acquired.

Another important unit implemented in the FEC is the Board Controller (BC). Based on a commercial FPGA, this circuit drives the ALTRO-bus transceivers and provides an independent access to the FEC via a separate serial link, the Local Slow Control (LSC). This secondary access is normally used to control the state of the voltage regulators and to monitor the board activity, power supplies and temperature. The maximum total power consumption per card is about 6W. In order to minimize the heat transfer to the detector sensitive volume, the FECs are embedded in two copper plates connected to a water cooling circuit.

As sketched in fig. 2, the FECs belonging to the same partition are connected to the Readout Control Unit [4] (RCU) via a PCB-based backplane, physically integrating both the ALTRO-bus and the LSC. Through the ALTRO-bus, the RCU broadcasts the trigger and clock information to the FECs, operates the initialization of the ALTROs and performs the readout of trigger related data. Completely independent of the operations with the ALTRO-bus, the RCU executes the monitoring and safety control functions via the LSC.

The RCU is interfaced with the ALICE Data Acquisition (DAQ) system, the Central Trigger Processor (CTP) and the Detector Control System (DCS) by means of two mezzanine cards: 1) the Detector Data Link Source Interface Unit (DDL SIU), which implements a full duplex 200MByte/s optical link and is the ALICE standard interface to the DAQ, and 2) the DCS/Trigger interface card. In particular, the latter incorporates the LHC TTCrx chip, through which it receives the clock and trigger information by the ALICE CTP, and the Detector Control System interface, with an embedded processor and an Ethernet interface.

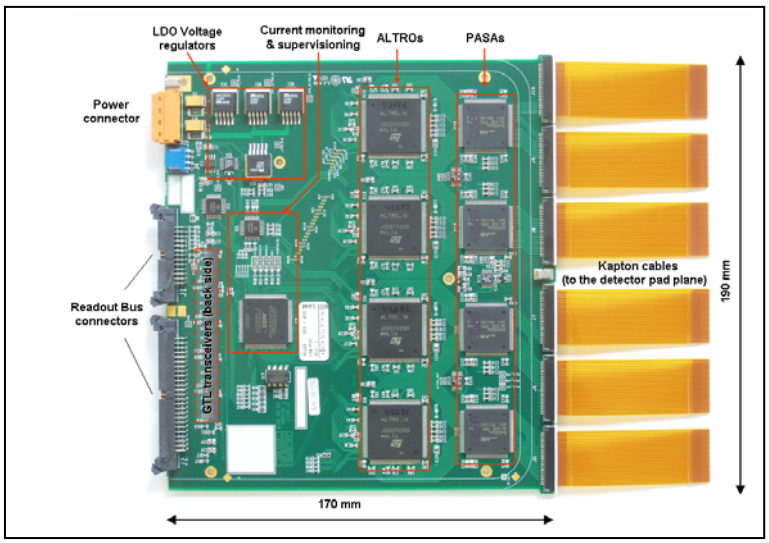

Figure 1: FEC layout. The components are mounted on both sides of the board. The figure shows the board topside with 4 PASAs, 4 ALTROs, the Board Controller for monitoring and supervisioning, the voltage regulators and other auxiliary components. On the bottom side of the board are symmetrically mounted 4 PASAs and 4 ALTROs and, close to the readout bus connectors, the transceivers for the ALTRO-bus interface.

The radiation load on the TPC is low (1krad $\oplus$ 10^{11}neutrons/cm^2 over 10 years). Thus radiation-soft technologies have been adopted for the implementation of the electronics. Nevertheless, some cares have been taken to protect the system against potential damages caused by Single Event Effects. Definitely, in addition to applying redundancy in the design of the most critical circuits, special solutions have been implemented to detect and cure possible upsets in the configuration of the programmable devices.

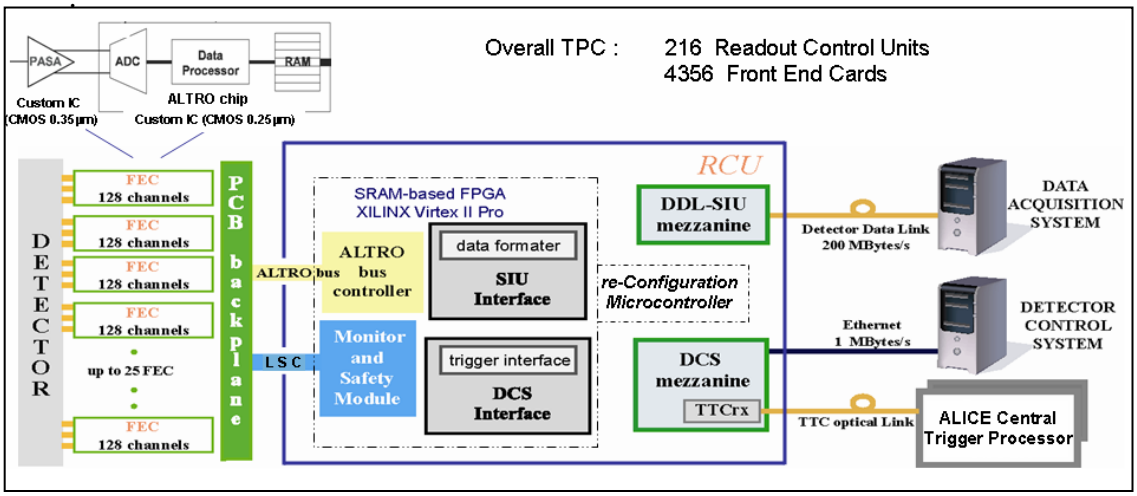

Figure 2: The architecture or the TPC readout electronics partition.

3. System performance

A fraction of the final electronics has been benchmarked by realistic measurements with a prototype of the ALICE TPC, proving that the system fulfils all design requirements. In particular, despite the high level of integration of digital circuits close to the analogue front-end, the system shows a noise figure of 730e^- (r.m.s.), almost 30% better than the design requirements. Moreover, the tests have shown that the system is able to process high multiplicity events with a baseline restoration at 1‰ of the dynamic range within 1μs (see fig.3)

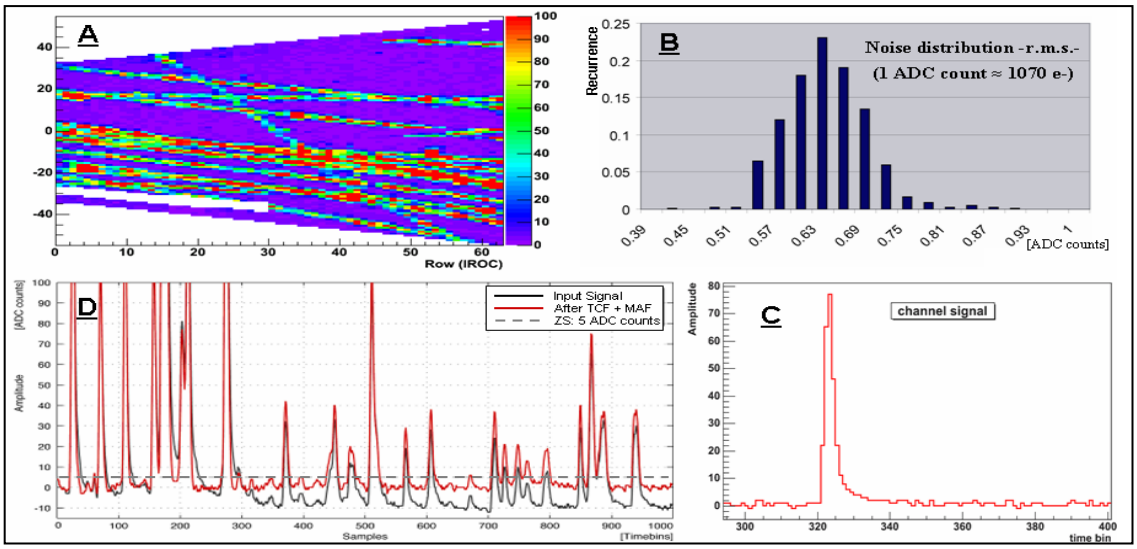

Figure 3: Processing of a high occupancy event (cosmic ray). The figure shows: A) the event tracks from the readout of a 5500 channels TPC prototype, B) the histogram of the r.m.s. noise, C) the shape of a single TPC pulse signal after the digitization and processing and D) the ALTRO signal processing performance: in black the signal at the input of the ALTRO chip processing chain; in red the combined effects of the ALTRO's Tail Cancellation filter (TCF) and Moving Average filter (MAF); the dotted line represents the zero suppression threshold. The application of the TCF and MAF allows retrieving signals that otherwise would be discarded by the zero suppression algorithm.

4. Conclusions

An innovative electronics system with on-detector signal processing has been developed for the ALICE TPC readout. A sizeable fraction of the final electronics has been successfully tested showing that the system fulfils all design requirements. The mass production of all the components (4356 FECs, 216 RCUs and the Readout Backplanes) has recently been completed. The installation on the detector is scheduled to start in spring 2006.

References:

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